

## PCB Layout and Design Considerations for CH7017 LVDS/TV Output Device

### 1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7017 LVDS/TV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for both LVDS and TV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures shown in this document are based on the 128-pin LQFP package of the CH7017 designed with an Intel Brookdale<sup>®</sup> / Intel Springdale<sup>®</sup> system.

### 2. Component Placement

Components associated with the CH7017 encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

#### 2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1 $\mu$ F ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7017 ground pins, in addition to ground vias.

##### 2.1.1 Ground Pins

The analog and digital grounds of the CH7017 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7017 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

##### 2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage VDDV), PLL, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

**Table 1: Power Supply Pins Assignment**

Pin #	# of pins	Type	Symbol	Description
118	1	Power	V5V	5V supply for H/VOOUT (5V)
64, 83, 84, 103	4	Power	DVDD	Digital Supply Voltage (3.3V)
67, 75, 92, 100	4	Power	DGND	Digital Ground
60	1	Power	VDDV	I/O Supply Voltage (1.1V to 3.3V)
55	1	Power	TVPLL_VDD	TV PLL Supply Voltage (3.3V)
54	1	Power	TVPLL_VCC	TV PLL Supply Voltage (3.3V)
51	1	Power	TVPLL_GND	TV PLL Ground
37	1	Power	DAC_VDD	DAC Supply Voltage (3.3V)
39, 48	2	Power	DAC_GND	DAC Ground
7, 13, 19, 20, 26, 32	6	Power	LVDD	LVDS Supply Voltage (3.3V)
4, 10, 16, 23, 29, 35	6	Power	LGND	LVDS Ground
1	1	Power	LPLL_VDD	LVDS PLL Supply Voltage (3.3V)
3	1	Power	LPLL_GND	LVDS PLL Ground

• **Digital, DAC and PLL Power Pins Decoupling and Connection**

Figure 1 shows the decoupling and connection for the LPLL\_VDD, LVDD, DAC\_VDD, TVPLL\_VCC, TVPLL\_VDD, DVDD and V5V.

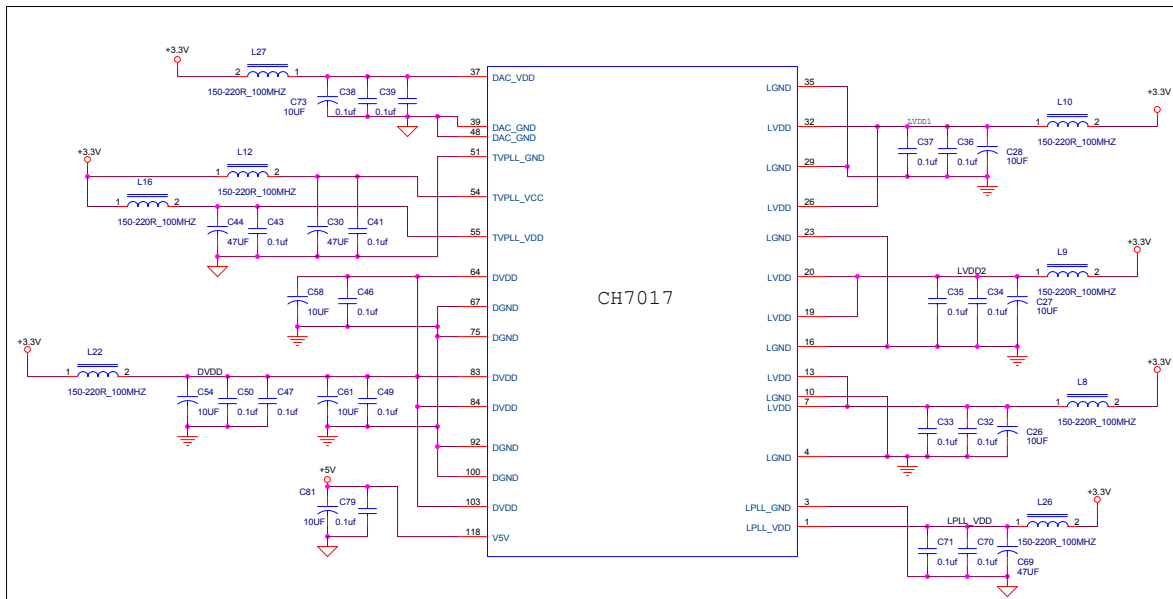


Figure 1: Digital, DAC and PLL Power pins Decoupling and Connection

**Note:** All the Ferrite Beads described in this document are recommended to have <math>.05 \Omega</math> at DC;

• **VDDV and VREF1, VREF2 Decoupling and Connection**

VDDV is the I/O supply voltage. This pin should be decoupled and connected to the maximum voltage level seen by the I/O of the CH7017 (1.1V to 3.3V).

VREF1 inputs a reference voltage of  $VDDV/2$ . The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, syncs and clock inputs. Please refer to **Figure 2** for the decoupling and connection.

VREF2 should be tied externally to the maximum voltage seen by the SDD, SDC, SPD and SPC ports (1.5V to 3.3V).

Figure 2 shows the decoupling and connection for VDDV, VREF1, and VREF2.

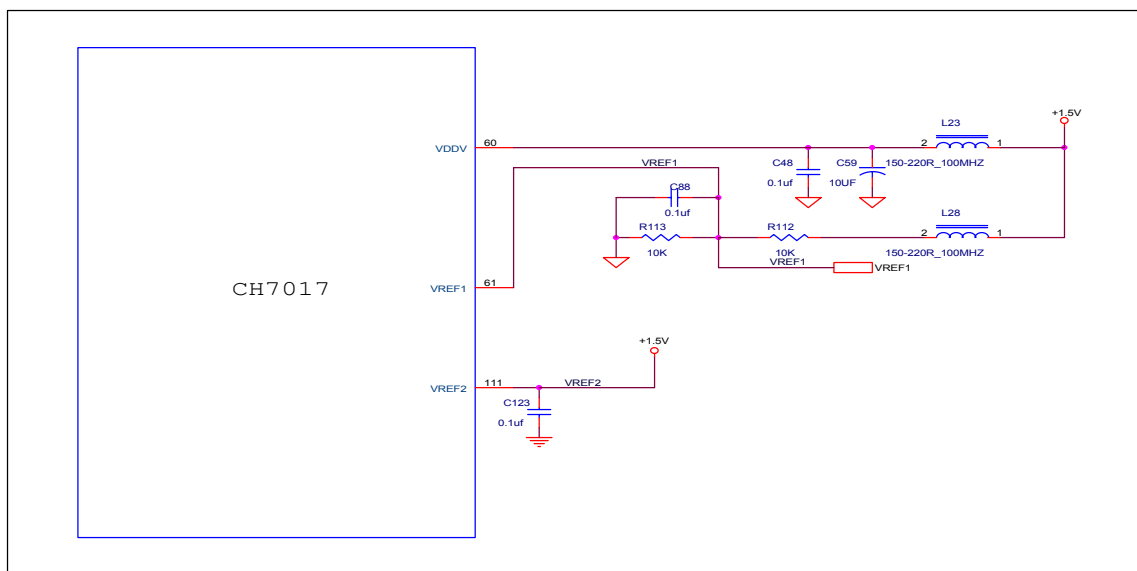


Figure 2: VDDV, VREF1, and VREF2 pins Decoupling and Connection

## 2.2 General Control

- **ISET Pin**

A 140 Ω resistor should be placed directly and as close as possible to Pin 38, ISET, with short and wide traces. Whenever possible, the ISET resistors ground pin should also be connected to pin 39, DAC ground. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7017. See **Figure 3** for design reference.

- **GPIO[5:0] Pins**

These pins provide general purpose I/O and are controlled via the serial port. The direction of the signals are controlled by register 6Eh, GPIO Direction Control Register. When the direction is “input”, the GPIO[5:0] pins have a weak pull-up (about 1 MΩ), and can be used to determine the type of panel, the standard/type of TV, etc., during system boot-up. See **Figure 3** for design reference. In the reference design, each GPIO pin is connected with a pair of resistors, which allow the designer to either pull-up or pull-down the pin. Using GPIO[0] (pin 123) as an example, if it should be set to HIGH, R71 can be stuffed with a 10 KΩ resistor, and R72 should be not stuffed. If it is to be set to LOW, then R71 should be not stuffed, and R72 can be stuffed with a 10 KΩ resistor.

- **AS pin**

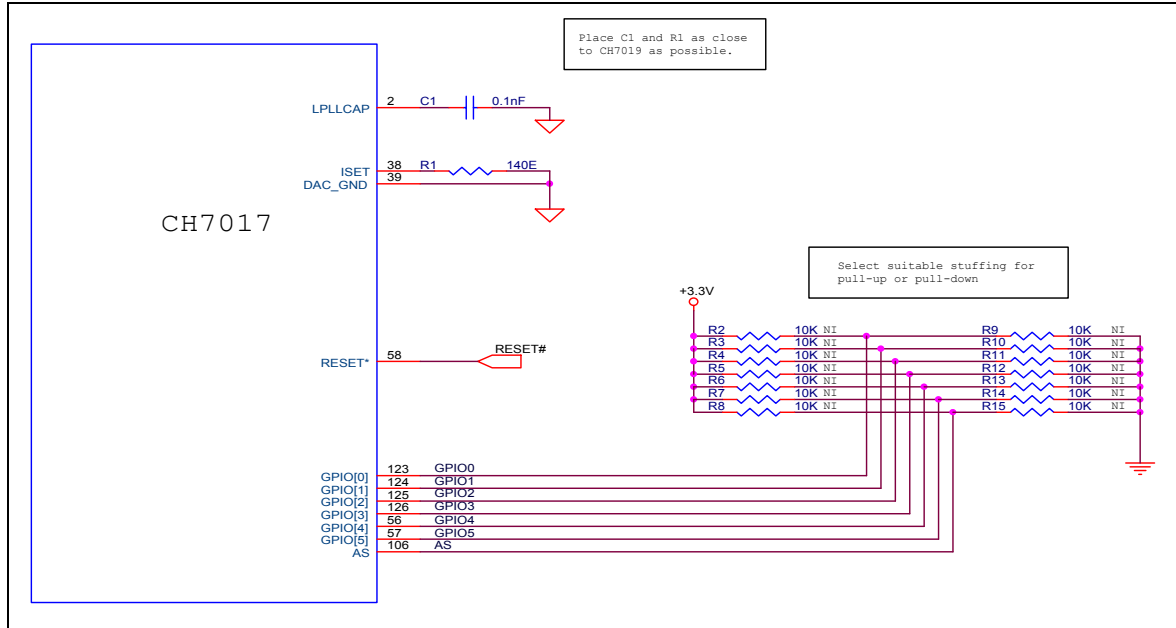
AS pin, which is internal pull-up, determines the device address of the CH7017 for the serial port. The device address is defined as {1 1 1 0 1 AS\* AS R/W}. With AS pulled low, the address is {1 1 1 0 1 1 0 R/W}, which is ECh (Write) or EDh (Read). With AS pulled high, the address is {1 1 1 0 1 0 1 R/W}, which is EAh (Write) or EBh (Read).

- **RESET\* pin**

RESET\* pin, which is internal pull-up, When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port. In the reference design, the pin is connected to RST\* of Intel’s DVO control.

- **LPLLCAP pin**

The LPLLCAP pin allows coupling of any signal to the on-chip loop filter capacitor. A capacitor with a typical value of 0.1 nF, should be connected between this pin (pin 2) and ground (See **Figure 3**).



**Figure 3: General Control Reference Design**

### 2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

Crystal Input

The 14.31818 MHz ( $\pm 20$ ppm) crystal must be placed as close as possible to the XI/FIN and XO pins (Pins 52 and 53), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7017 encoder, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent to these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7017 pin 51 ground.

**Reference Crystal Oscillator**

The CH7017 includes an oscillator circuit which allows a 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7017. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value ( $C_L$ ).

External load capacitors have their ground connection very close to the CH7017 ( $C_{ext}$ ).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each has approximately 10 pF ( $C_{int}$ ) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$$

where:

$C_{ext}$  = external load capacitance required on XI/FIN and XO pins.

$C_L$  = crystal load capacitance specified by crystal manufacturer.

$C_{int}$  = capacitance internal to CH7017 (approximately 10-15 pF on each of XI/FIN and XO pins).

$C_S$  = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 4** for the symbols used in the calculation described above.

In general, let us assume

$$C_{int \text{ XI/FIN}} = C_{int \text{ XO}} = C_{int}$$

$$C_{ext \text{ XI/FIN}} = C_{ext \text{ XO}} = C_{ext}$$

such that

$$C_L = (C_{int} + C_{ext}) / 2 + C_S \quad \text{and} \quad C_{ext} = 2(C_L - C_S) - C_{int}$$

$$= 2C_L - (2C_S + C_{int})$$

Therefore  $C_L$  must be specified greater than  $C_{int} / 2 + C_S$  in order to select  $C_{ext}$  properly.

After  $C_L$  (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to AN-06.

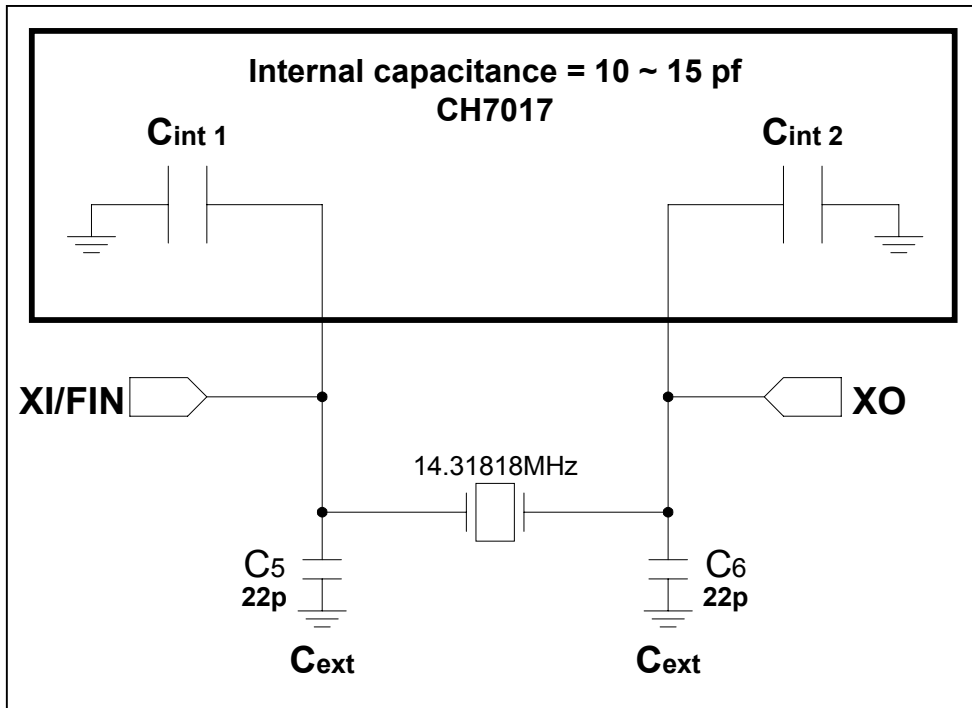


Figure 4: Reference Crystal Design.

- **P-Out pin**

The P-Out pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output driver is driven from the VDDV supply (pin 60). In the reference design, this pin is connected to DVOBC\_CLKIN (DVO clock input). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.

- **XCLK1, XCLK1\*, XCLK2, XCLK2\* (External Clocks Input) pins**

XCLK1 and XCLK1\* form a differential clock signal input to CH7017 for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1\* input should be connected to VREF1. In the reference design they are connected to DVOB\_CLK and DVOB\_CLK# (see Figure 5 for reference design).

XCLK2 and XCLK2\* form a differential clock signal input to CH7017 for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2\* input should be connected to VREF1. In the reference design they are connected to DVOC\_CLK and DVOC\_CLK# (see Figure 5 for reference design).

- **BCO/VSYNC pin**

Pin 50, the BCO/VSYNC pin, provides either a buffered clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply. When it is used as a buffered clock out, the BCO register (register 22h) controls the types of the output clocks (see CH7017 datasheet for details). It is very useful for troubleshooting. See TB-37 for the methods of measuring crystal clock and color burst frequencies using BCO pin.

For the reference design of the clock pins, please see Figure 5.

- **C/HSYNC pin**

Pin 49, the C/HSYNC pin, provides either a composite sync for TV modes or a horizontal sync for RGB bypass mode. This pin is driven by the DVDD supply.

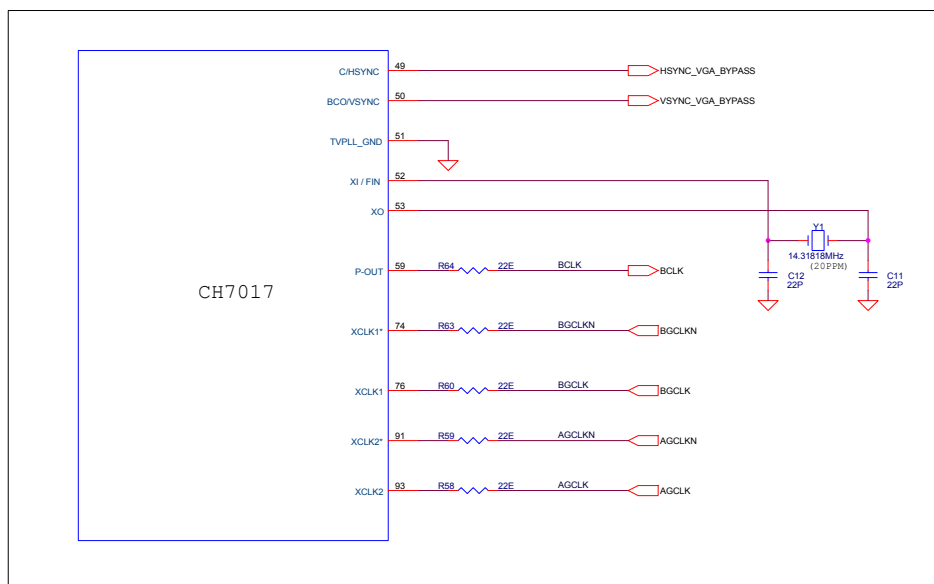


Figure 5: Clock and Crystal Oscillator Reference Design

## 2.4 Serial Ports Control

- **SPD and SPC pins**

SPD (pin 107) and SPC (pin 108) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 1 KΩ resistors and are connected to MI2C\_DATA and MI2C\_CLK, respectively.

- **SDD and SDC pins**

SDD and SDC pins (pins 112 and 113) are for low-voltage DDC serial data and clock. In the reference design, they are connected to either DVI\_DATA, DVI\_CLK or DDC\_DATA, DDC\_CLK of DVO ports.

- **DD1 and DC1 pins**

DD1 and DC1 (pins 114 and 115) are a pair of serial data and clock for DDC (0V to 5.0V). In the reference design, they are pulled up to +5.0V and are used to transfer VGA monitor information.

- **DD2 and DC2 pins**

DD2 and DC2 (pins 116, 117) are a second pair of serial data and clock for DDC (0V to 5.0V). In the reference design, they are pulled up to +5.0V and are used to transfer LVDS panel information.

See **Figure 6** for serial ports control reference design.

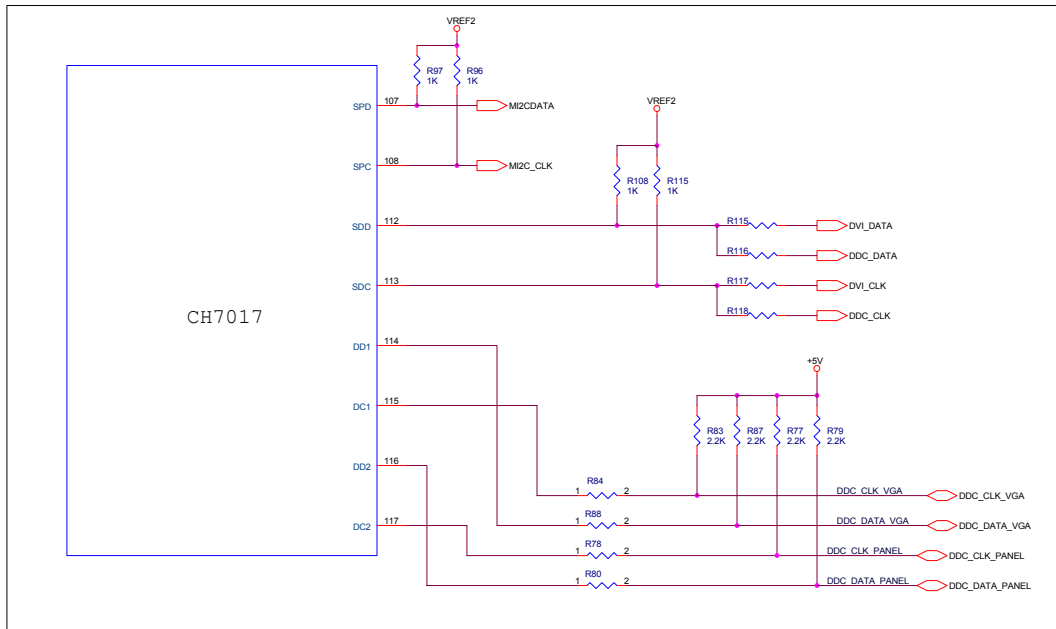


Figure 6: Serial Port Control Reference Design

## 2.5 Data Input and Syncs

Since the digital pixel data and the pixel clock of the CH7017 may toggle at speeds of up to 165MHz (depending on the input mode), it is critical that the connection of these video input signals between the graphics controller and the CH7017 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

- **D1[11:0] and D2[11:0]**

Each set of data pins accept a set of 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level. The two sets of data pins can be ganged together as a single 24 bit data port. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used when routing these signals.

- **H1 and V1**

When the SYO control bit is low, these pins accept horizontal/vertical sync inputs for use with the D1[11:0] input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs.

- **H2 and V2**

When the SYO control bit is low, these pins accept a horizontal/vertical sync inputs for use with the D2[11:0] input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs.

- **Hin and Vin**

These pins are the inputs of the voltage translating digital buffer. The input threshold can be for Hin and Vin is either VREF2/2 or DVDD/2, depending on the setting of the HVIBS register, reg. 52h - bit 5.

- **Hout and Vout**

These pins are the outputs of the voltage translating digital buffer and are driven from the V5V power rail.

Figure 7 shows the reference design example for data input and syncs.

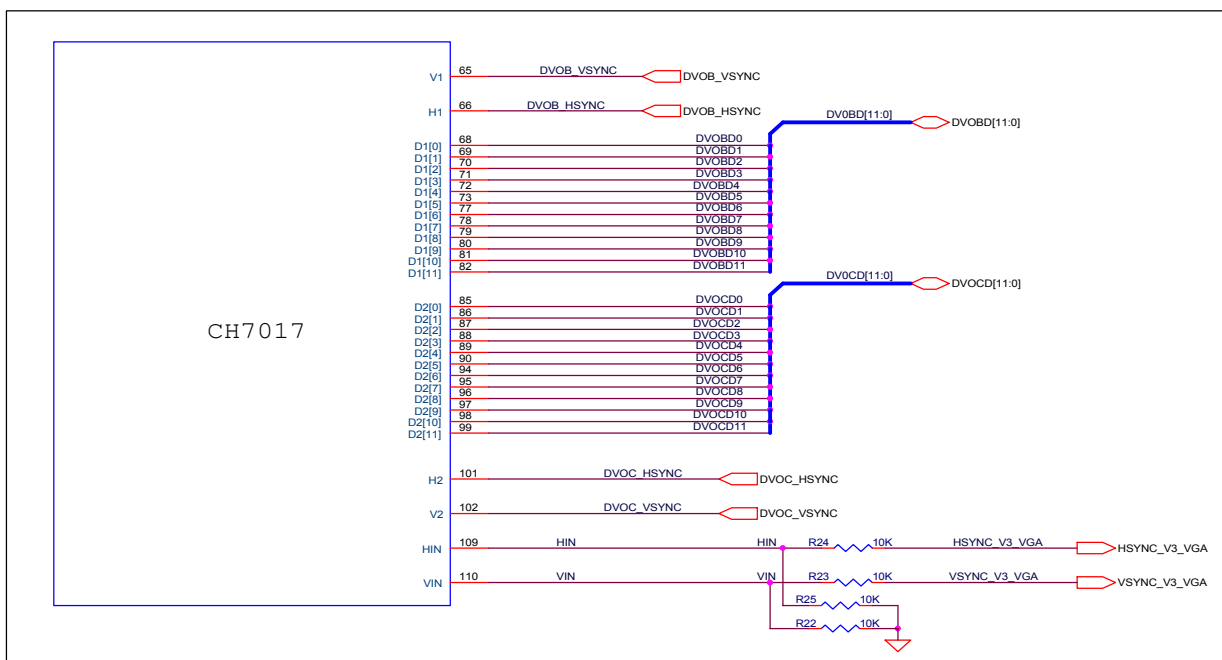


Figure 7: Data Input and Syncs Reference Design

## 2.6 TV Output and Control

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7017 from the graphics controller’s digital output port. A P-OUT clock can be outputted as the reference frequency to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7017 from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. **Figure 8** shows the design example for TV out and control.

The components associated with the video output pins should be placed as close as possible to the CH7017. The 75 Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7017 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs or Y, Pr and Pb signals should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit elements for a typical S-Video and composite outputs are shown in **Figure 9**, and its corresponding frequency response is shown in **Figures 10 and 11**.

The four TV encoder DAC outputs can be switched to two sets of output pins DACA[3:0] and DACB[3:0] via video switches. This feature facilitates simple connection to two sets of video connectors as listed in **Table 2**.

**Table 2: TV Output Configurations**

	<b>2 RCA + 1 S-Video</b>	<b>SCART</b>
<b>DACA0 (pin 47)</b>	CVBS	B
<b>DACA1 (pin 43)</b>	Y	G
<b>DACA2 (pin 45)</b>	C	R
<b>DACA3 (pin 41)</b>	CVBS	CVBS
	<b>VGA – Bypass RGB</b>	<b>HDTV</b>
<b>DACB0 (pin 46)</b>	B	Pb
<b>DACB1 (pin 42)</b>	G	Y
<b>DACB2 (pin 44)</b>	R	Pr

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on one set of DAC output pins, different reconstruction filters for each type of signals can be implemented on the break-out cables. **Figure 12** shows the connection for the SCART output.

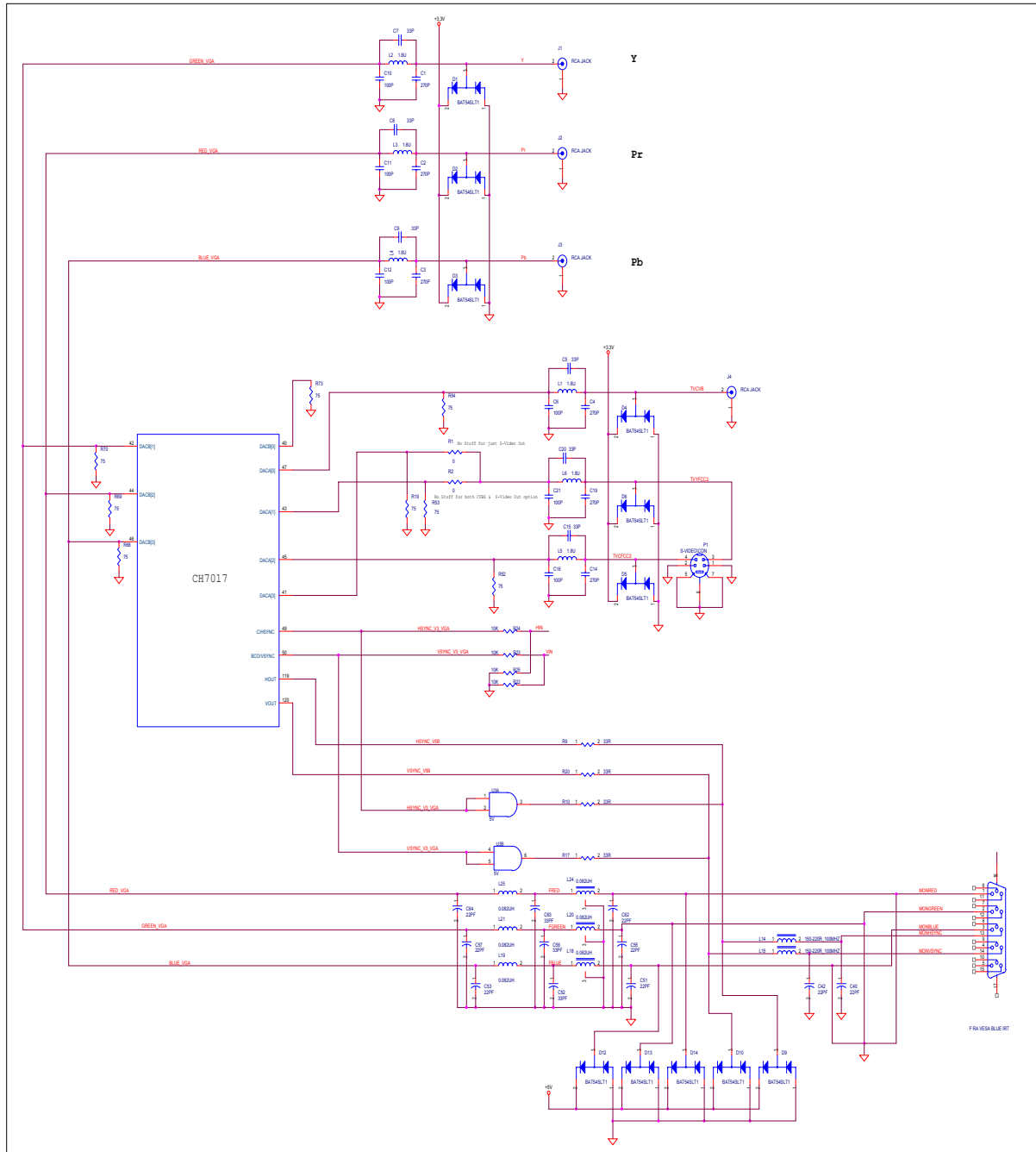
Bits 5 and 6 of Register 73h, LPCPC: LDAS0 and LDAS1 control the DAC analog switch according to the description shown on **Table 3**.

**Table 3: TV DAC Analog Switch Control**

<b>LDAS1</b>	<b>LDAS0</b>	<b>DACA path</b>	<b>DACB path</b>
0	0	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On

When RGB bypass mode is selected, pin 49, C/HSYNC, and pin 50, BCO/VSYNC, provide horizontal sync and vertical sync, respectively, for the RGB display monitor.

**In order to minimize the hazard of ESD, a set of protection diodes MUST BE used for each DAC connecting to TV (Refer to AN-38 for details).**



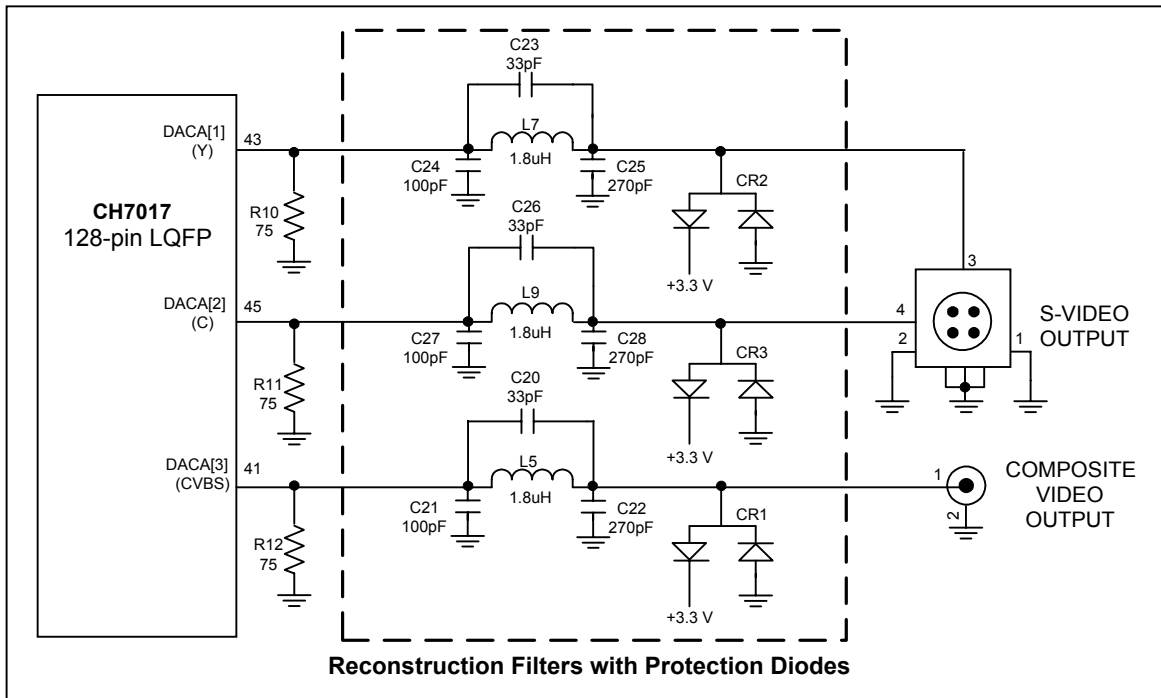


Figure 9: The Typical Connection For the S-Video and Composite Outputs

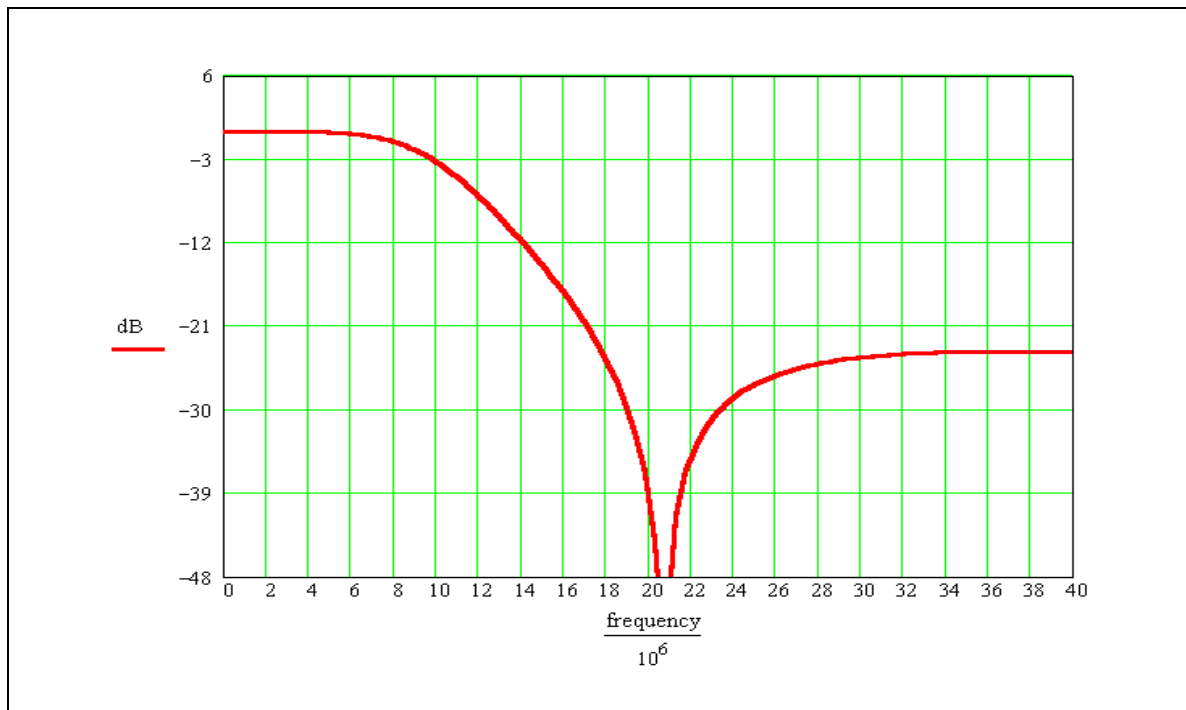


Figure 10: S-video and Composite Output Amplitude Response of the 3<sup>rd</sup> Order Reconstruction Filter as shown in Figure 9.

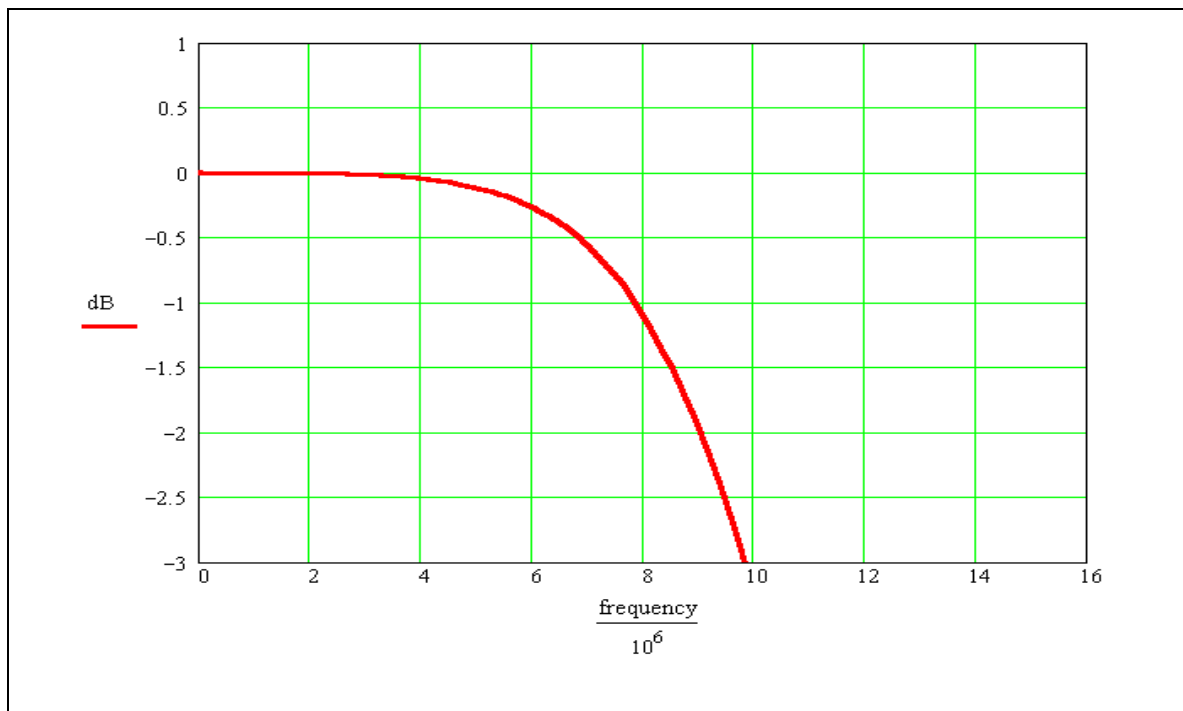


Figure 11: The Details of the Amplitude Response of the Pass Band

**Note:** If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN-46 on how to achieve the desired configuration.

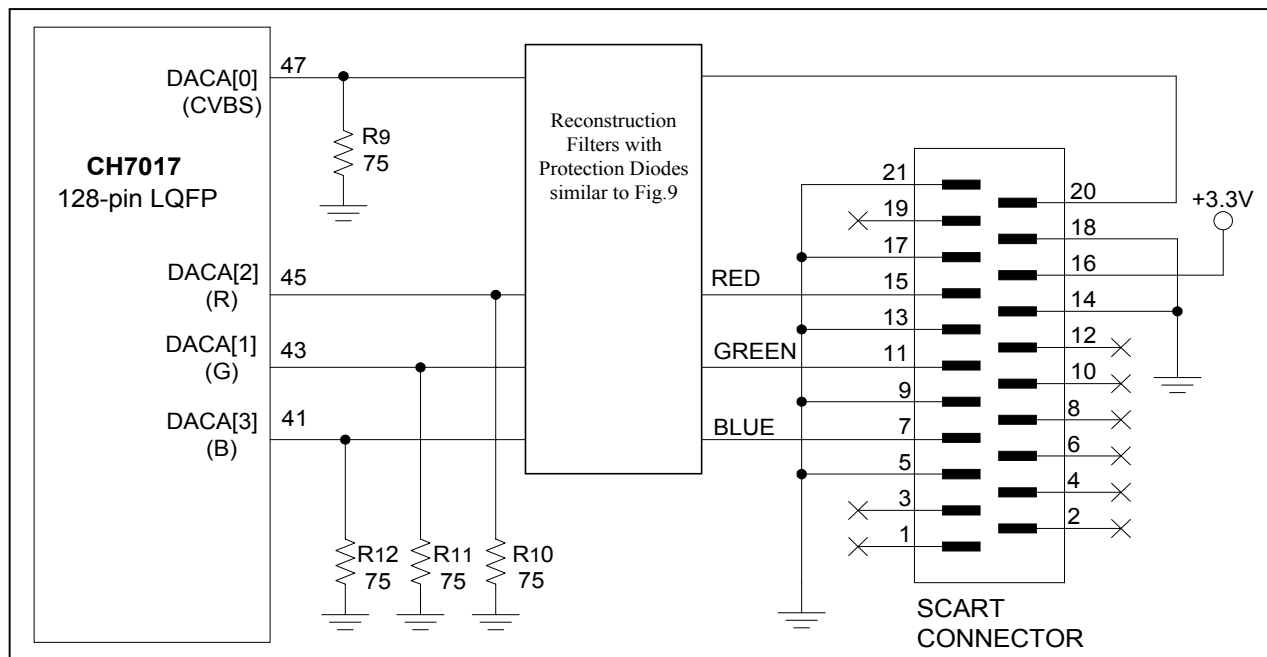


Figure 12: The Connection for the SCART Connector

Careful layout consideration for the CVBS, Y and C (or CVBS, R, G and B) traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

## 2.7 LVDS Output and Control

The LVDS output pins include: LDC[7:0], LL1C, LL1C\*, LL2C, LL2C\*. The LVDS control pins include: VSWING, FLD/STL1, FLD/STL2, DE1, DE2, ENAVDD, ENABKL, HPD and HPINT\*. The connection of these pins are described as follows. **Figure 13** shows a reference design example for LVDS output and control.

- **VSWING**

VSWING is the LVDS swing control. This pin sets the swing level of the LVDS outputs. A 2.4 K $\Omega$  resistor should be connected between this pin and LGND (pin 35) using short and wide traces.

- **FLD/STL1, FLD/STL2**

These outputs can be programmed to be either a TV Field output from the TV encoder or a Stall output from the flat panel Up-scaler. These outputs are tri-stated upon power-up. In the reference design, the two pins are connected directly to Intel's DVOB\_FLD/STL and DVOC\_FLD/STL respectively.

- **HPD, HPINT\***

HPD, Hot Plug Detect pin (pin121) determines whether a display device is connected to the VGA connector. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT\* (Hot Plug Interrupt, pin 122) pin pulling low. In the reference design, the HPINT\* is connected to Intel's DVOBC\_INTR#.

- **DE1, DE2**

DE1 and DE2 are Data Enable control pins for Channel 1 and Channel 2, respectively.

These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF1 is the threshold level. The reference design, these pins are connected to Intel's DVOB\_BLANK# and DVOC\_BLANK#, respectively.

- **ENAVDD, ENABKL**

ENAVDD (pin127) and ENABKL (pin 128) are for LVDS panel power control: ENAVDD enables the panel's 3.3V VDD and ENABKL enables the panel's back-light. In the reference design, these pins are connected to the panel's VDD and backlight control circuits respectively.

- **LDC[7:0], LL1C, LL1C\*, LL2C, LL2C\***

The LDC[7:0], LL1C, LL1C\*, LL2C, LL2C\* signals are high frequency differential signals that need to be routed with special precautions. They must be routed in pairs with the length as close as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the connector without any vias to the bottom layer. Trace for the LVDS signals should be closely coupled and the trace should be 100 $\Omega$  differential impedance (50 $\Omega$  to the ground from each differential pin).

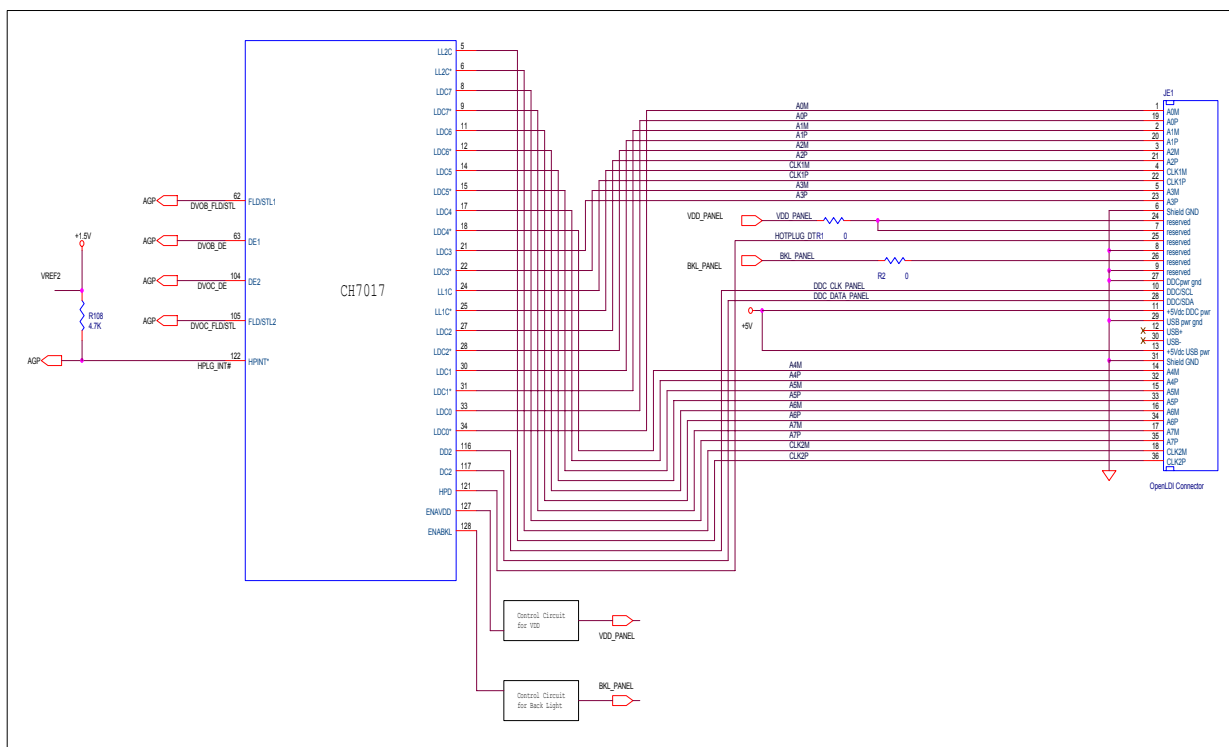


Figure 13: LVDS Output and Control Reference Design

### 3. LVDS Output Design Tips

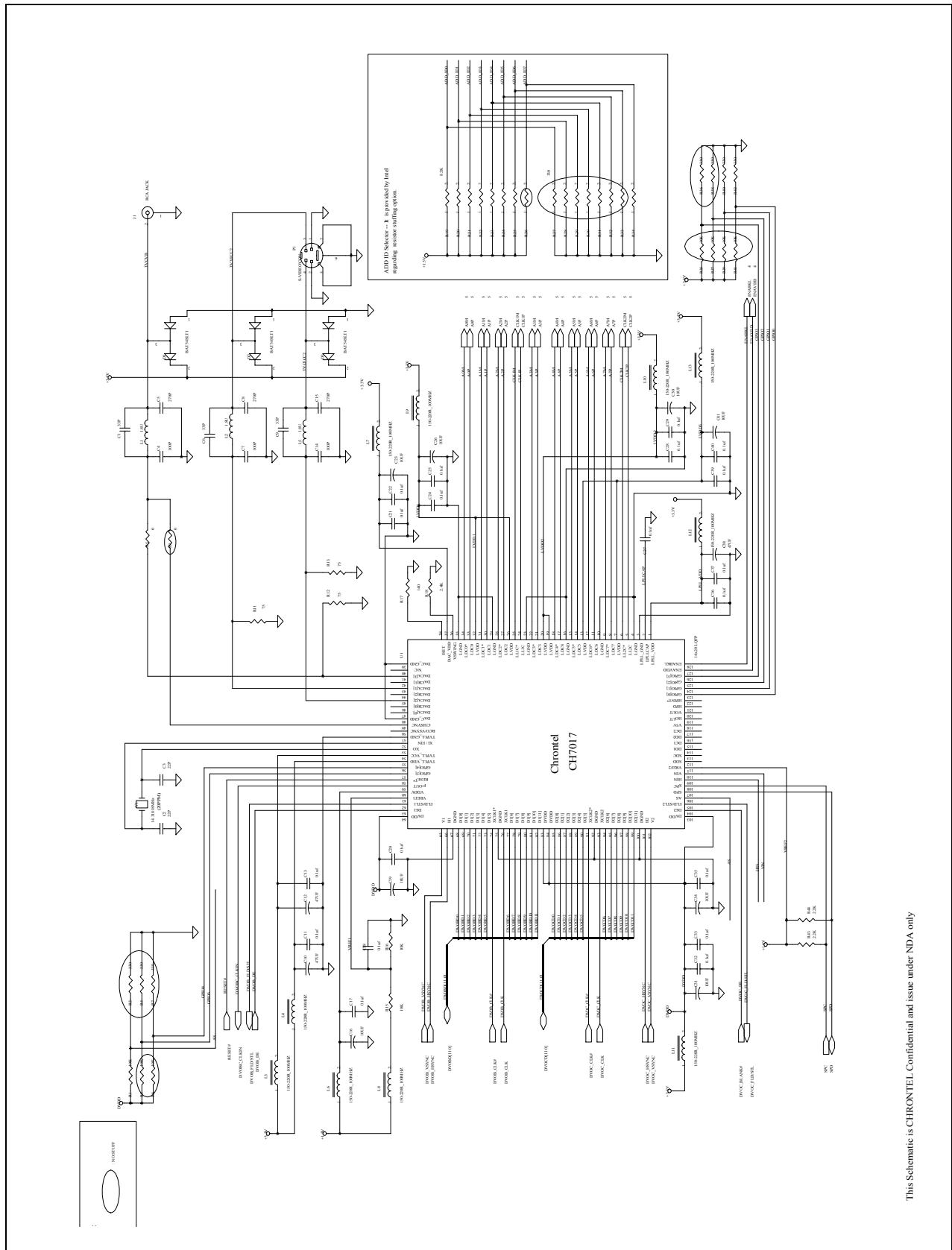
#### Output and Control Reference Design

- Dedicating planes for Vcc and Ground are typically required for high-speed design. The solid ground plane is required to establish a controlled impedance for the transmission line interconnects. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance.
- If it is possible, put CMOS/TTL signals and LVDS signals on a different layers which should be isolated by the power and ground planes.
- Power and ground should use wide (low impedance) traces. Do not use 50Ω design rules on power and ground traces.
- Keep ground PCB return paths short and wide. Provide a return path that creates the smallest loop for the image currents to return.
- Traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance. This not only reduces EMI, but also helps to ensure noise coupled onto the conductors will be common-mode noise.
- Leave all unused LVDS and CMOS/TTL output open. Do not tie them to ground.
- Tie unused transmitter inputs and control/enable signals to power or ground.

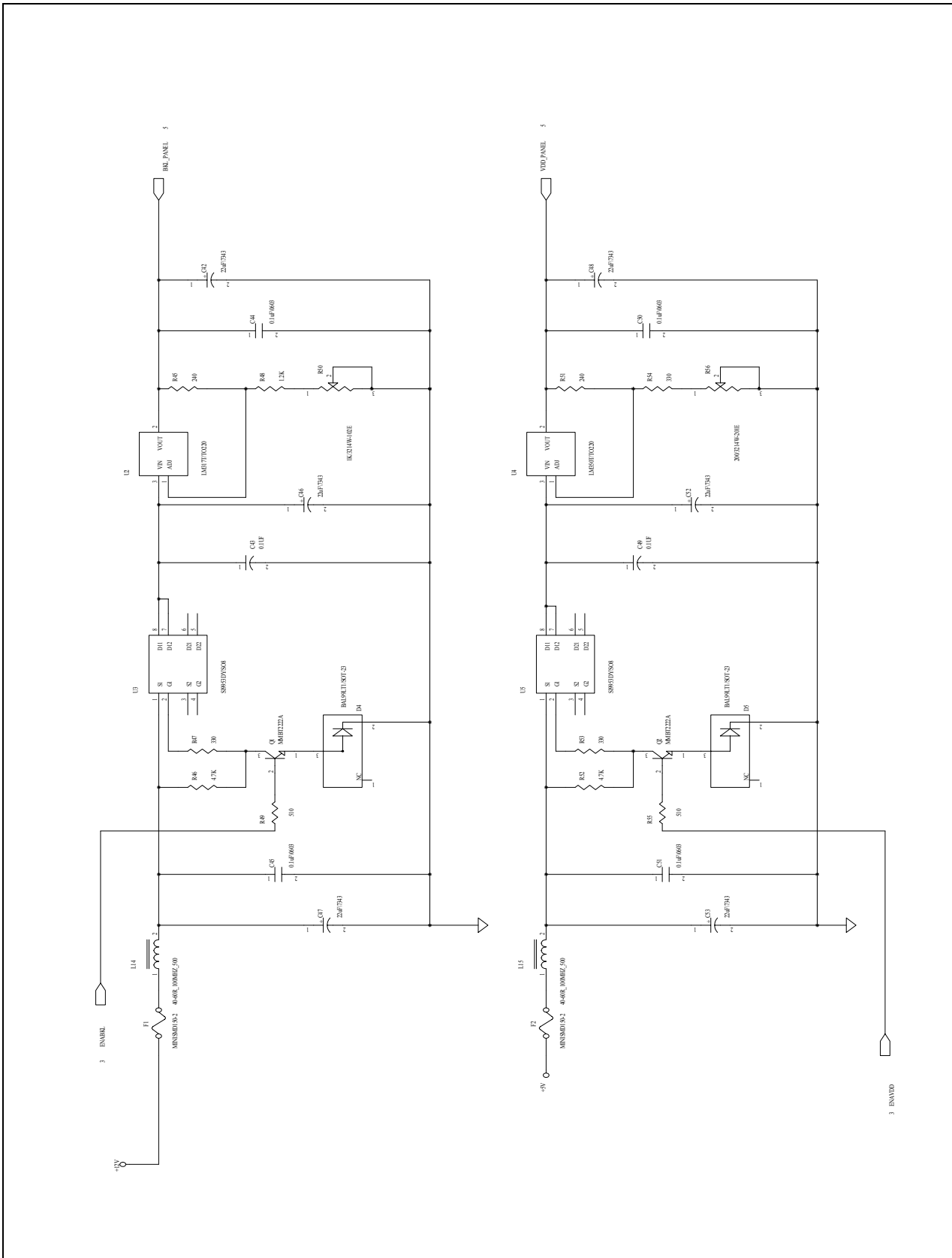
## **4. Reference Design Example**

The following schematic are given to be used as a CH7017 PCB design example only. It is not a complete design. Those who are seriously doing an application design with CH7017 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

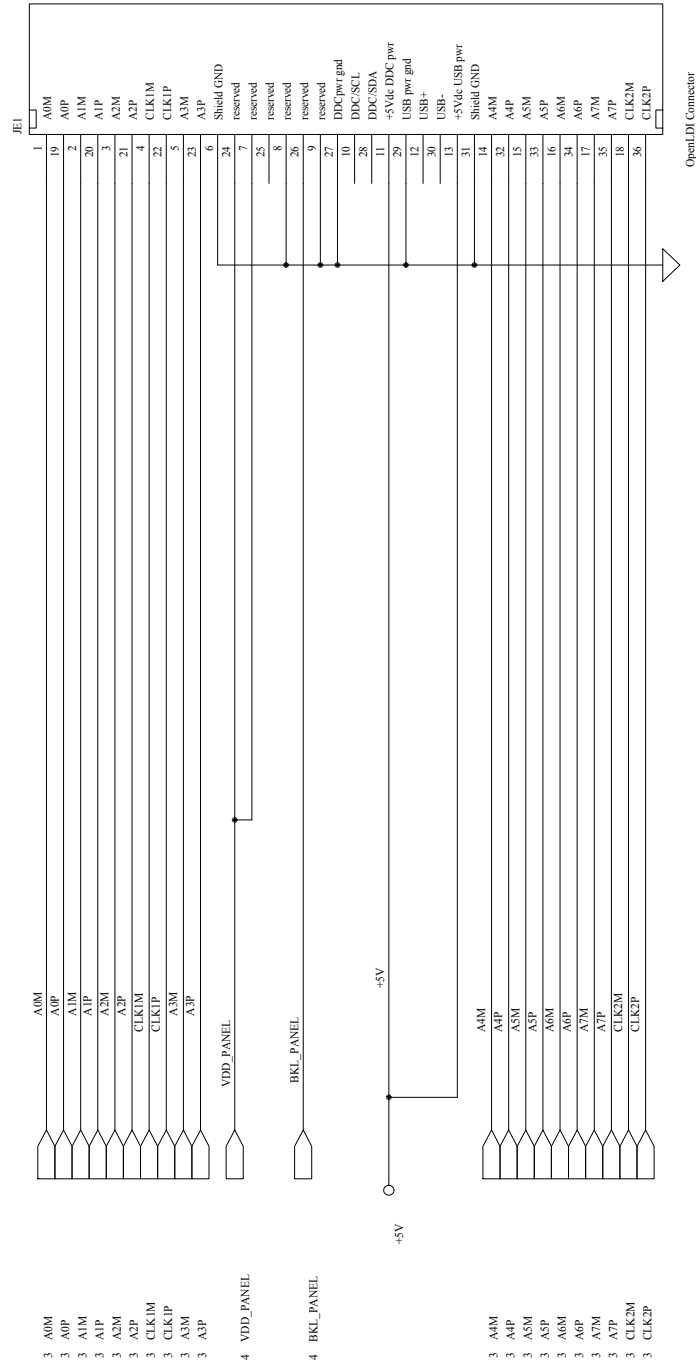
### **4.1 Schematics of Reference Design Example**



This Schematic is CHRONTEL Confidential and issue under NDA only



Open LDI Connector



## 5. Revision History

Rev. #	Date	Section	Description
1.0	11/15/01	All	First official release.
1.1	3/1/02	All, 4.1	Replaced the Almador <sup>®</sup> based reference schematics with a Brookdale <sup>®</sup> / Springdale <sup>®</sup> based reference schematics. All figures are changed according the new reference schematics. All references to the new figures have been updated.
		4.1	PCB Layout and BOM removed.
1.2	12/20/02	2.1.2	Pin count corrected for TVPLL VDD in Table 1.
		2.6	Table 2 corrected. Figure 10, 11, and 12 updated.
		5.0	Document Revision History added
1.3	8/28/03	All	DACA[3], DACA[0] pin number fix. These pins corresponds to pin 41 and pin 43 respectively.
		2.6	Schematics updated.

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