Chrontel

# AN-55

**Application Notes**

# PCB Layout and Design Considerations for the CH7205 DVD/TV Encoder

## 1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7205 DVD/TV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for TV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures shown in this document are based on the 48-pin LQFP package of CH7205 designed with a Swan ES4408 DVD Processor.

## 2. Component Placement

Components associated with the CH7205 encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

### 2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7205 ground pins, in addition to ground vias.

#### 2.1.1 Ground Pins

The analog and digital grounds of the CH7205 should be separate but eventually connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7205 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

#### 2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage VDDV), PLL, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

**Table 1: Power Supply Pins Assignment**

| Pin # | # of pins | Type | Symbol | Description |
|---|---|---|---|---|
| 5, 16, 33 | 3 | Power | DVDD | Digital Supply Voltage (3.3V) |
| 8, 18, 31, 39 | 4 | Power | DGND | Digital Ground |
| 41 | 1 | Power | VDDV | I/O Supply Voltage (1.1V to 3.3V) |
| 34 | 1 | Power | AVDD | PLL Supply Voltage (3.3V) |
| 37 | 1 | Power | AGND | PLL Ground |
| 28 | 1 | Power | VDD | DAC Supply Voltage (3.3V) |
| 19, 26 | 2 | Power | GND | DAC Ground |

- **Digital, DAC and PLL Power Pins Decoupling and Connection**

  **Figure 1** shows the decoupling and connection for the DVDD, AVDD, and VDD.

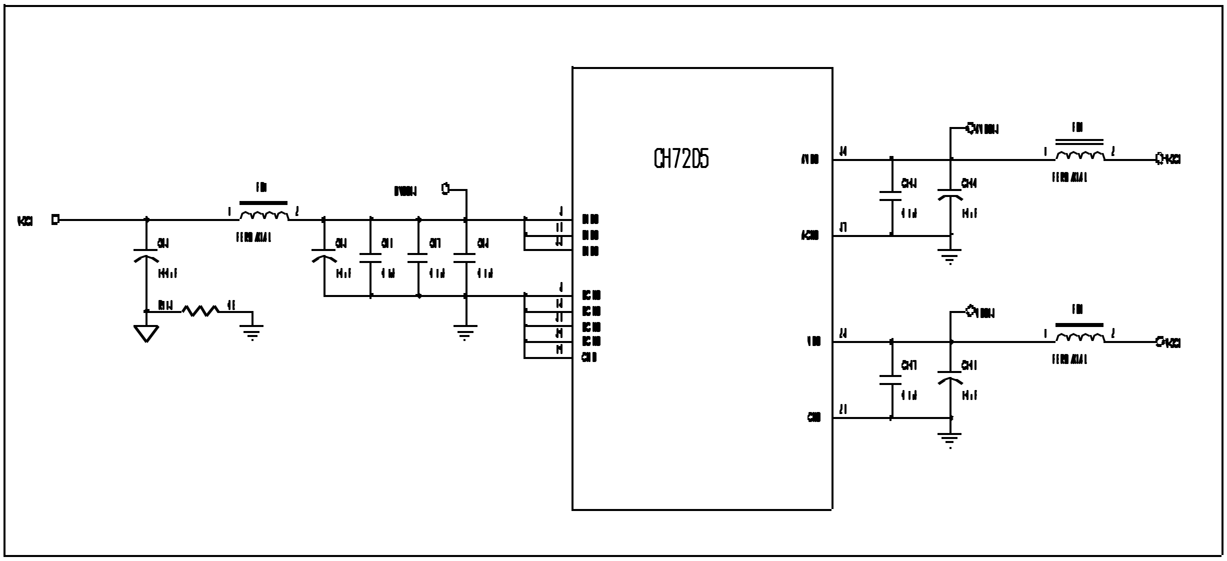



**Figure 1: Digital, DAC and PLL Power pins Decoupling and Connection**

**Note:** All the Ferrite Beads described in this document are recommended to have <.05 Ω at DC; 2 3Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair-Rite part# 2743019447 for detail or an equivalent part can be used for the diagram.

## • VDDV and VREF Decoupling and Connection

VDDV is I/O supply voltage (1.1V to 3.3V), which makes the amplitude of I/O signals from 0V to VDDV.

VREF inputs a reference voltage of VDDV/2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, syncs and clock inputs. Please refer to **Figure 2** for the decoupling and connection.

**Figure 2** shows the decoupling and connection for the VDDV, and VREF.

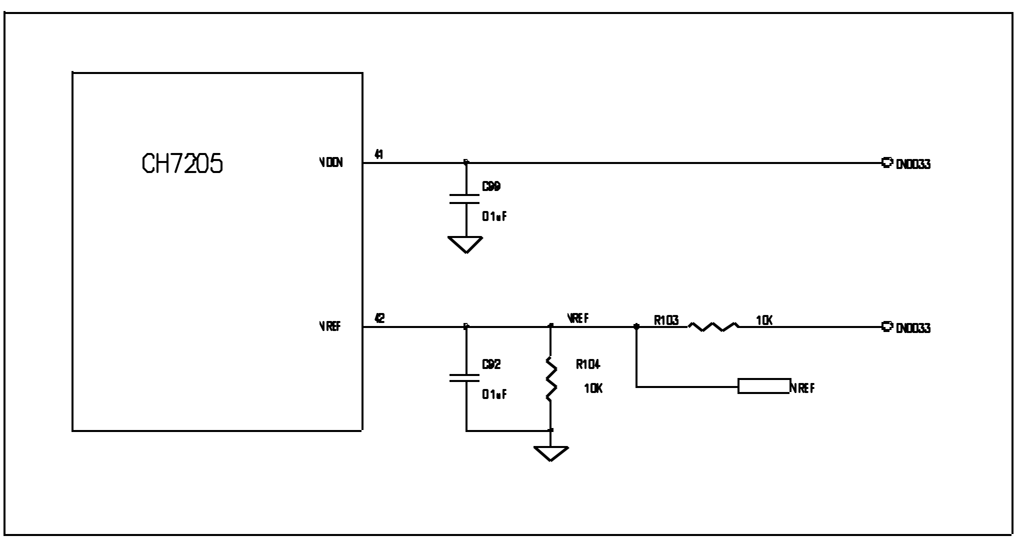



**Figure 2: VDDV, VREF1, and VREF2 pins Decoupling and Connection**

## 2.2 General Control

- **ISET Pin**

A 140 Ω resistor should be placed directly and as close as possible to Pin 27, ISET, with short and wide traces. Whenever possible, the ISET resistors ground pin should also be connected to pin 26, DAC ground (GND). Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7205. See **Figure 3** for design reference.

- **GPIO[1:0] Pins**

These pins provide general purpose I/O and are controlled via the serial port. The direction of these signals are controlled by register 1Eh, GPIO Control Register. When the direction is "input", the GPIO[1:0] pins have a weak pull-up (about 1 MΩ), and can be used to determine the type of panel, the standard/type of TV, etc., during system boot-up. See **Figure 3** for design reference. In the reference design, each GPIO pin is connected with a pair of resistors, which allows the designer to either pull-up or pull-down the pin. Using GPIO[0] (pin 14) as an example, if it should be set to HIGH, R108 can be stuffed with a 10 KΩ resistor, and R110 should not be stuffed. If it is to be set to LOW, then R108 should not be stuffed, and R110 can be stuffed with a 330Ω resistor.

- **RESET* pin**

The RESET* pin has an internal pull-up. When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

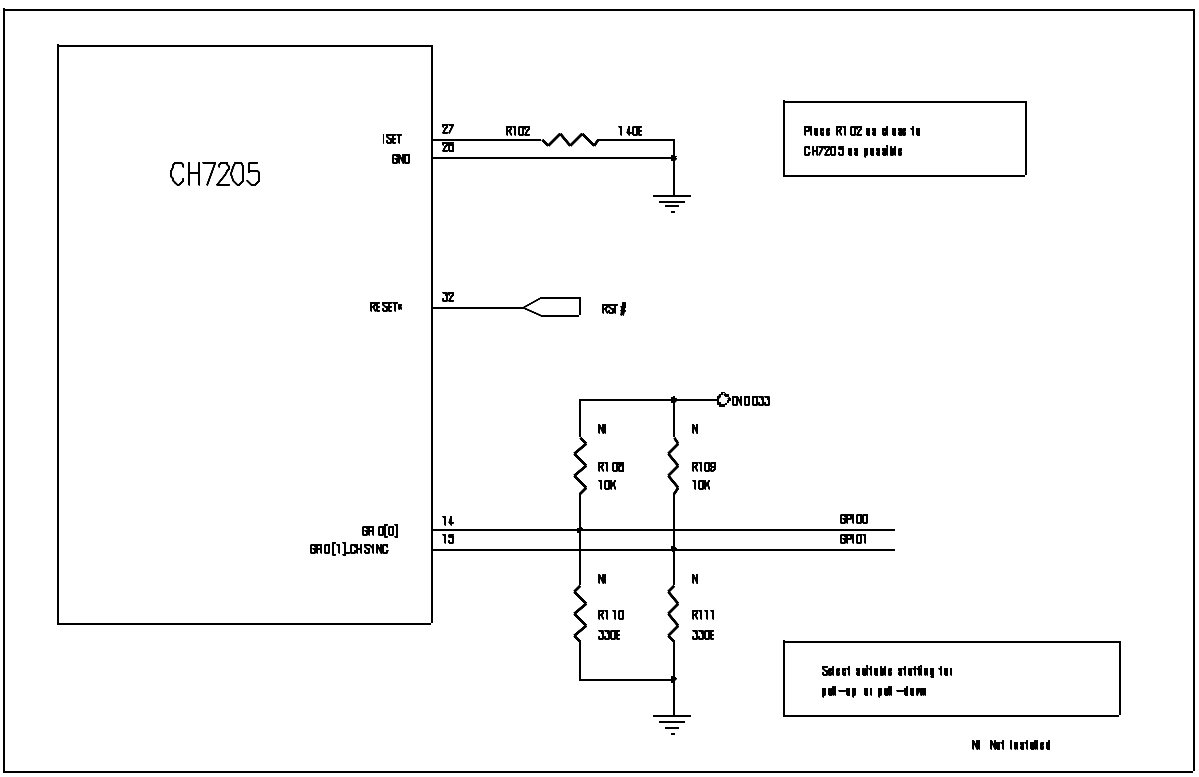



**Figure 3: General Control Reference Design**

## 2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

### Crystal Input

The 14.31818 MHz (±20ppm) crystal must be placed as close as possible to the XI/FIN and XO pins (Pins 35 and 36), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7205 encoder, it is very important that noise does not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7205 pin 34 ground pin.

### Reference Crystal Oscillator

The CH7205 includes an oscillator circuit which allows a 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7205. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and posse low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal required is specified to be 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value ($C_L$).

External load capacitors must have their ground connection very close to the CH7205 ($C_{ext}$).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each has approximately 10 pF ($C_{int}$) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$\mathbf{C_{ext} = (2 \times C_L) - C_{int} - 2C_S}$$

where:

$C_{ext}$= external load capacitance required on XI/FIN and XO pins.

$C_L$= crystal load capacitance specified by crystal manufacturer.

$C_{int}$= capacitance internal to CH7205 (approximately 10-15 pF on each of XI/FIN and XO pins).

$C_S$ = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 4** for the symbols used in the calculation described above.

In general, let us assume

$C_{int}$ XI/FIN = $C_{int}$ XO = $C_{int}$

$C_{ext}$ XI/FIN = $C_{ext}$ XO = $C_{ext}$

such that

$C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int}$

$= 2 C_L - (2C_S + C_{int})$

Therefore $C_L$ must be specified greater than $C_{int}/2 + C_S$ in order to select $C_{ext}$ properly.

After $C_L$ (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is **not** operating in an excessive drive level specified by crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For a detail consideration of crystal oscillator design, please refer AN-06.

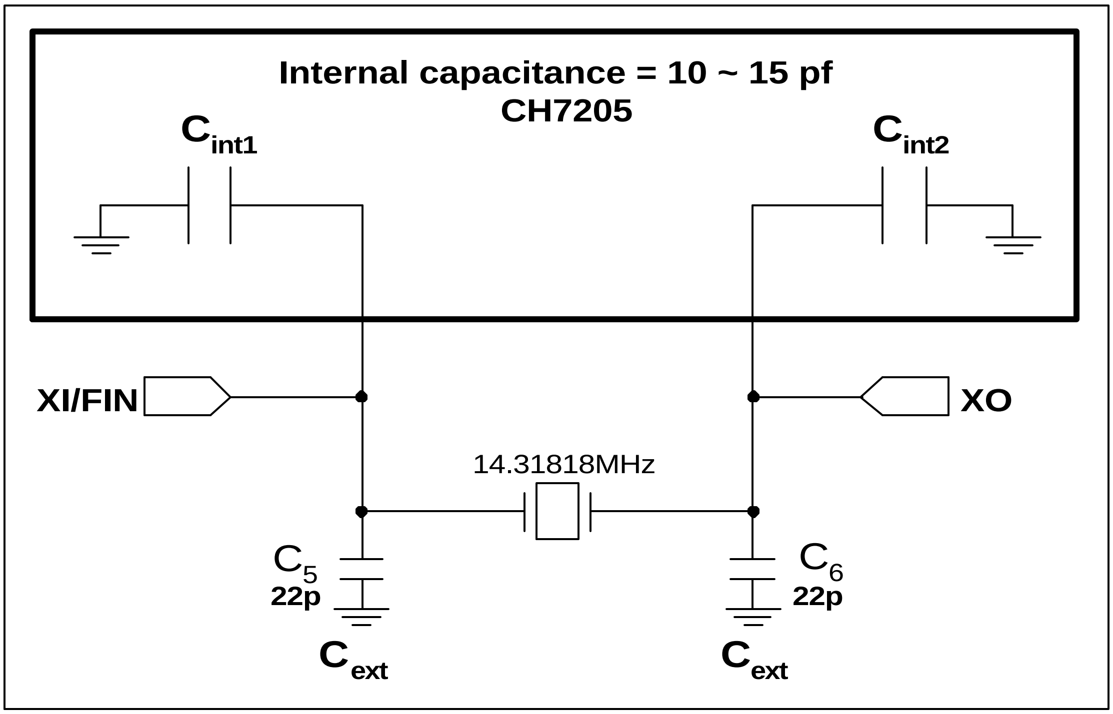



**Figure 4: Reference Crystal Design**.

- **P-Out pin**

The P-Out pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output driver is driven from the VDDV supply (pin 41). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.

- **XCLK, XCLK* (External Clocks Input) pins**

XCLK and XCLK* form a differential clock signal input to CH7205 for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. In the reference design they are connected to ADCLK and VREF (see **Figure 5** for reference design).

- **BCO (Buffered Clock Output) pin**

BCO pin (pin 38) provides buffered crystal oscillator clock output. This pin is driven by the DVDD supply. The BCO register (register 22h) controls the types of the output clocks (see CH7205 datasheet for details). It is very useful for troubleshooting. See TB-37 for the methods of measuring crystal clock and color burst frequencies using BCO pin.

For the reference design of the clock pins, please see **Figure 5**.

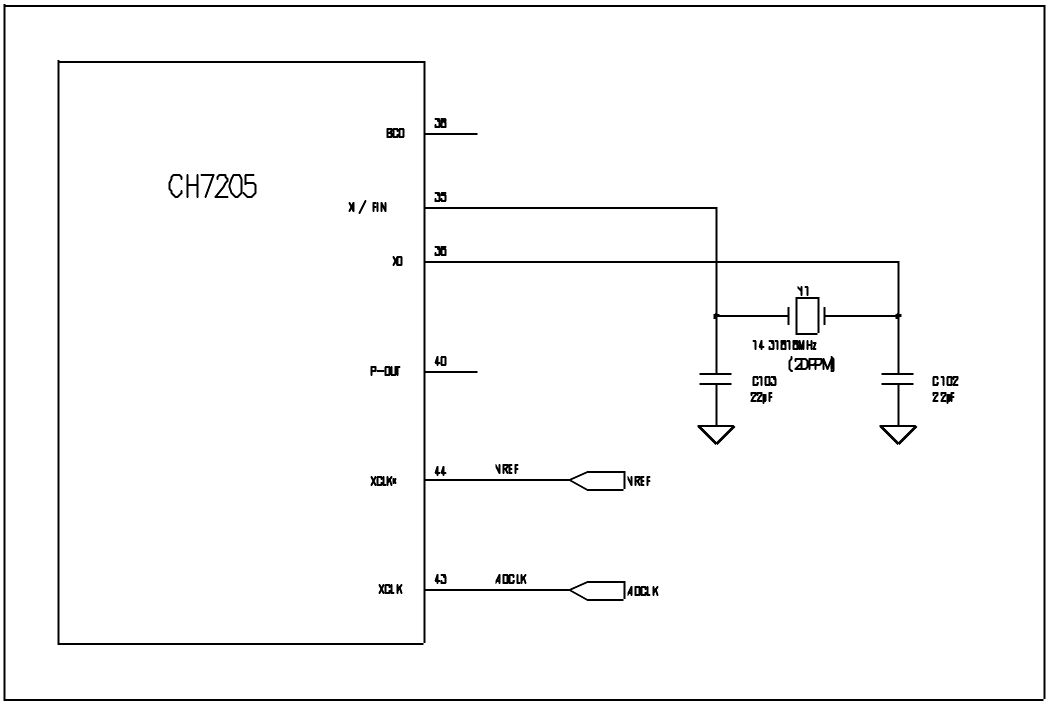



**Figure 5: Clock and Crystal Oscillator Reference Design**

## 2.4 Serial Port Control

- **SPD and SPC pins**

SPD (pin 29) and SPC (pin 30) functions as a bi-directional serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 2.2 KΩ resistors and are connected directly to AUX0 and AUX1, respectively.

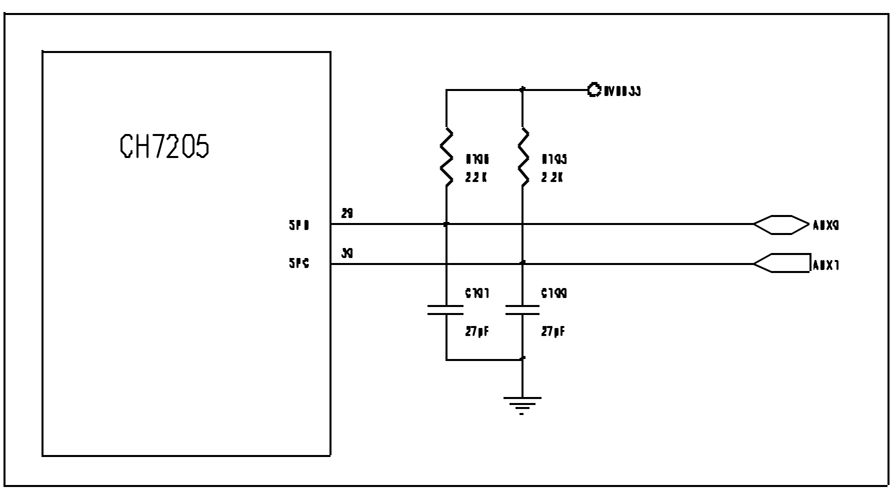



**Figure 6: Serial Port Control Reference Design**

## 2.5 Data Input and Syncs

Since the digital pixel data and the pixel clock of the CH7205 may toggle at speeds of up to 165MHz (depending on the input mode), it is critical that the connection of these video input signals between the graphics controller and the CH7205 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

- **D[11:0]**

  These data pins accepts up to 12 bits of data input from a digital video port. The levels are 0V to **VDDV**. VREF is the threshold level. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that the trace width of these signals be 8 mils.

- **H and V**

  When the SYO control bit is low, these pins accepts horizontal/vertical sync inputs for use with the D[11:0] input data. The amplitude will be 0V to **VDDV**. VREF is the threshold level for these inputs.

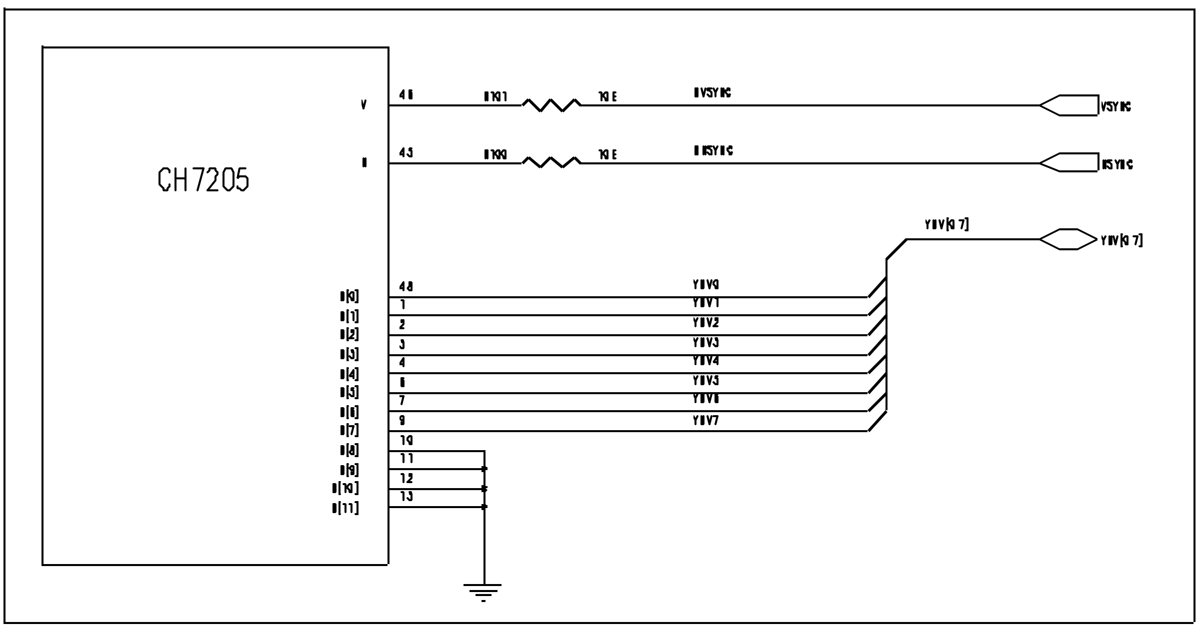



**Figure 7: Data Input and Syncs Reference Design**

- **Embedded Sync Mode**

In order to enable this mode, the Input Data Format Register, reg. 1Fh, needs to be set for IDF = 4. Although, the HSYNC and VSYNC signals can be embedded into the data stream, it is recommended that the H and V pins (pin 45 and pin 46 respectively) be pulled low with a 10KΩ resistor. Please refer CCIR656 for details on how the HSYNC and VSYNC, odd field & even field signals are generated within the data stream (See **Figure 8** for more design details for embedded sync in slave clock mode. Please note that the master clock mode can also be used.)

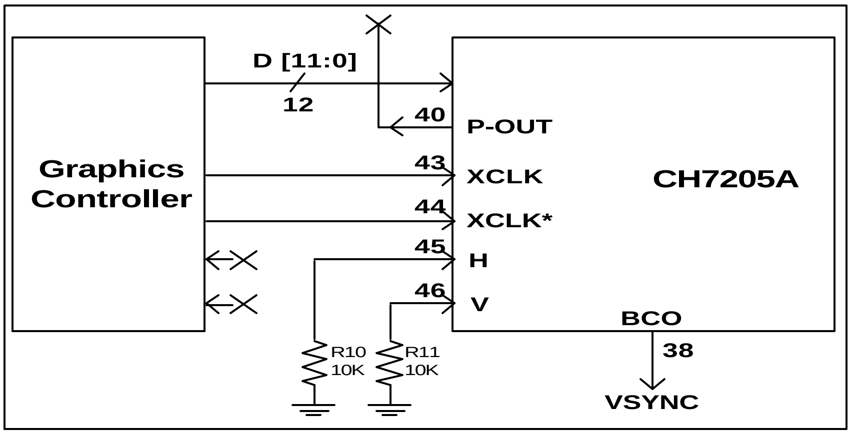



**Figure 8: Embedded Sync (in slave clock) Mode**

## 2.6 TV Output and Control

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7205 from the graphics controller's digital output port. A P-OUT clock can be outputted as the frequency reference to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7205 from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. **Figure 9** shows the design example for TV out and control.

The components associated with the video output pins should be placed as close as possible to the CH7205. The 75 Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7205 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs or Y, Pr and Pb signals should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit elements for a typical S-Video and composite outputs are shown in **Figure 10**, and its corresponding frequency response is shown in **Figure 11 and 12**.

**Table 2: TV Output Configurations**

| | **2 RCA + 1 S-Video** | **SCART** |
|---|---|---|
| **DACA0 (pin 17)** | CVBS | CVBS |
| **DACA1 (pin 25)** | Y | G |
| **DACA2 (pin 23)** | C | R |
| **DACA3 (pin 21)** | CVBS | B |
| | **SDTV** | |
| **DACA0 (pin 17)** | CVBS | |
| **DACB1 (pin 24)** | Y | |
| **DACB2 (pin 22)** | Pr | |
| **DACB3 (pin 20)** | Pb | |

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on the set of DAC output pins, different reconstruction filters for each type of signals can be implemented on the break-out cables. **Figure 12** shows the connection for the SCART output.

**In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each DAC connecting to TV (Refer to AN-38 for details).**

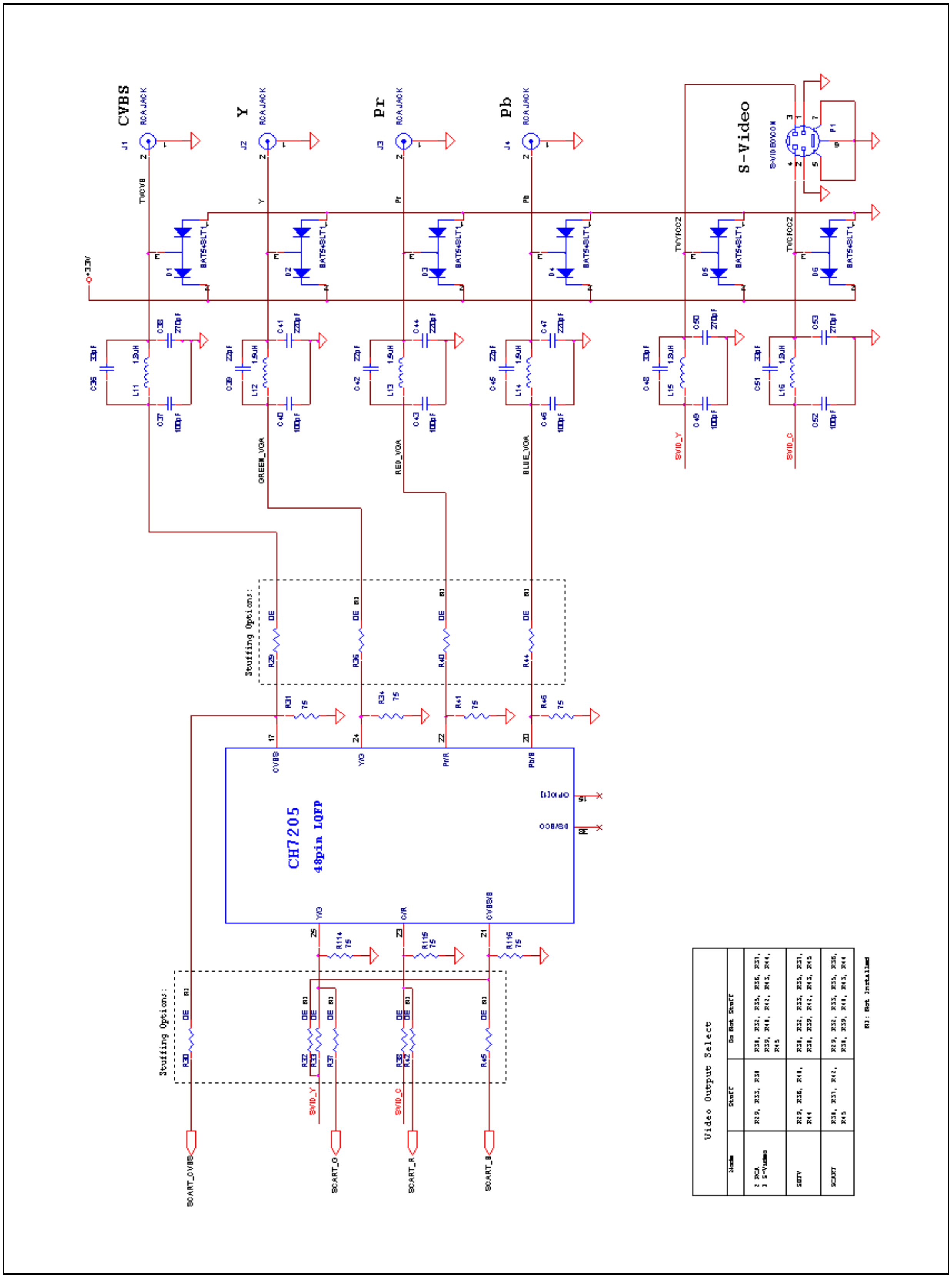



Figure 9: TV Output and Control Reference Design

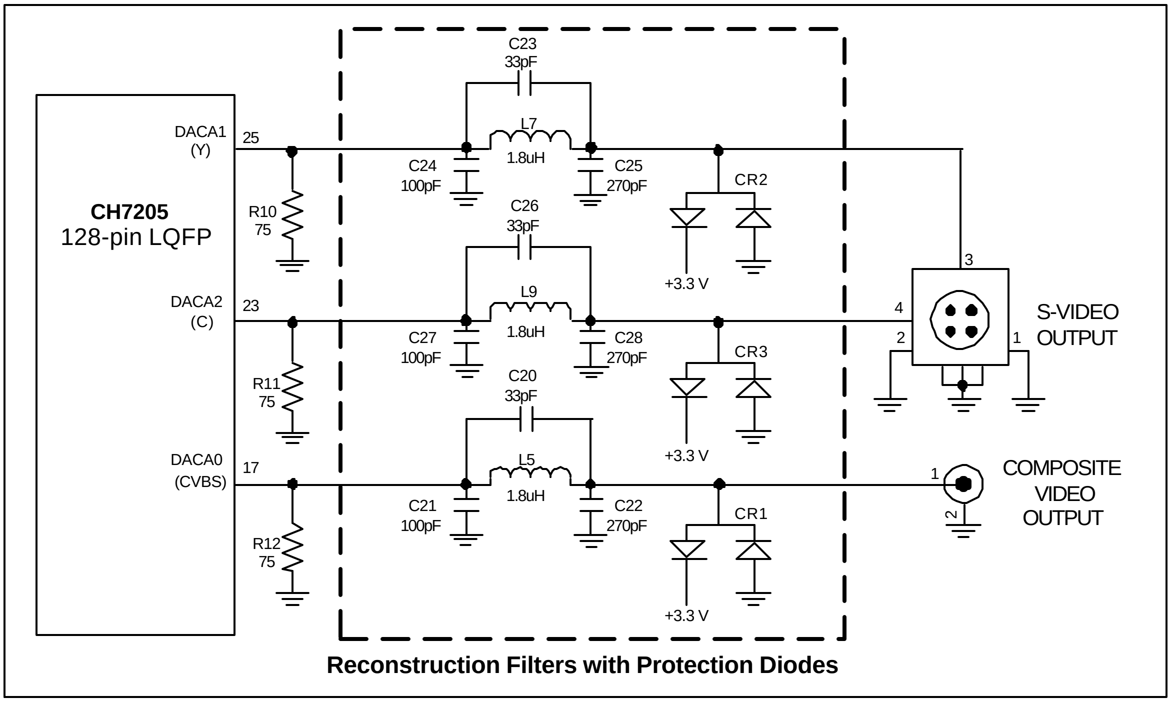



**Figure 10: The Typical Connection For the S-Video and Composite Outputs**

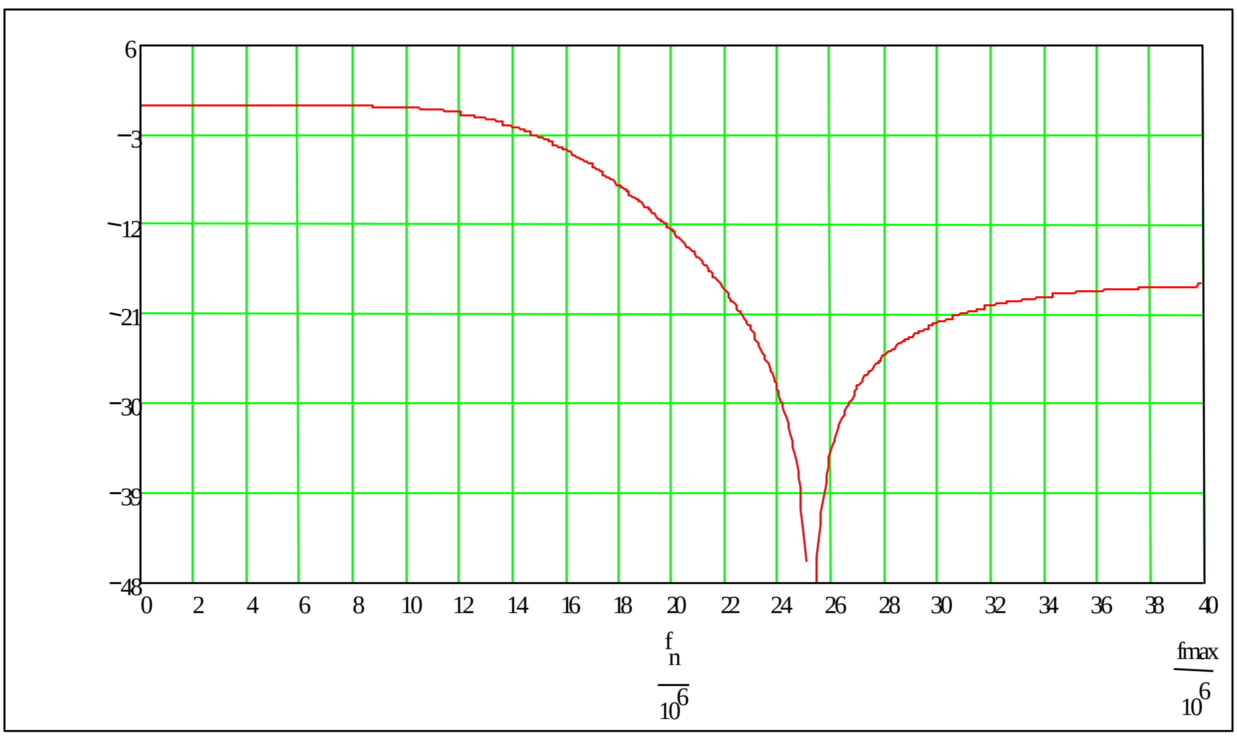



**Figure 11: Amplitude Response of the 3rd Order Reconstruction Filter**

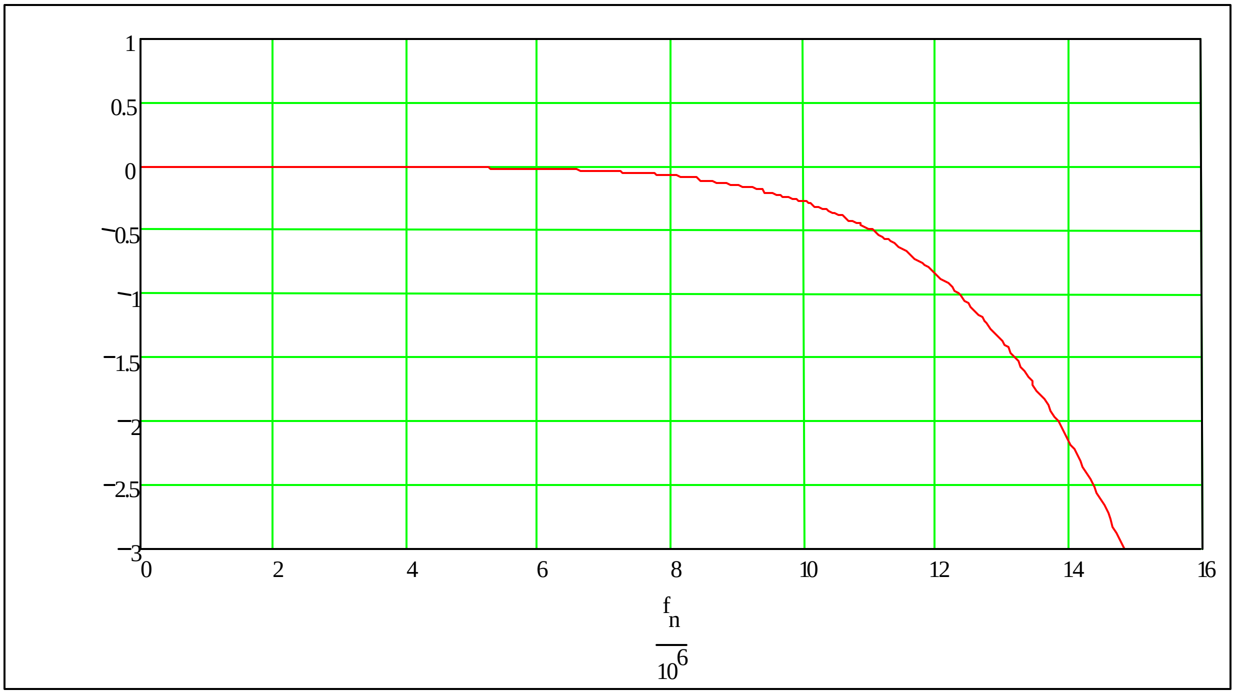



**Figure 12: The Details of the Amplitude Response of the Pass Band**

**Note:** If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN-46 on how to achieve the desired configuration.

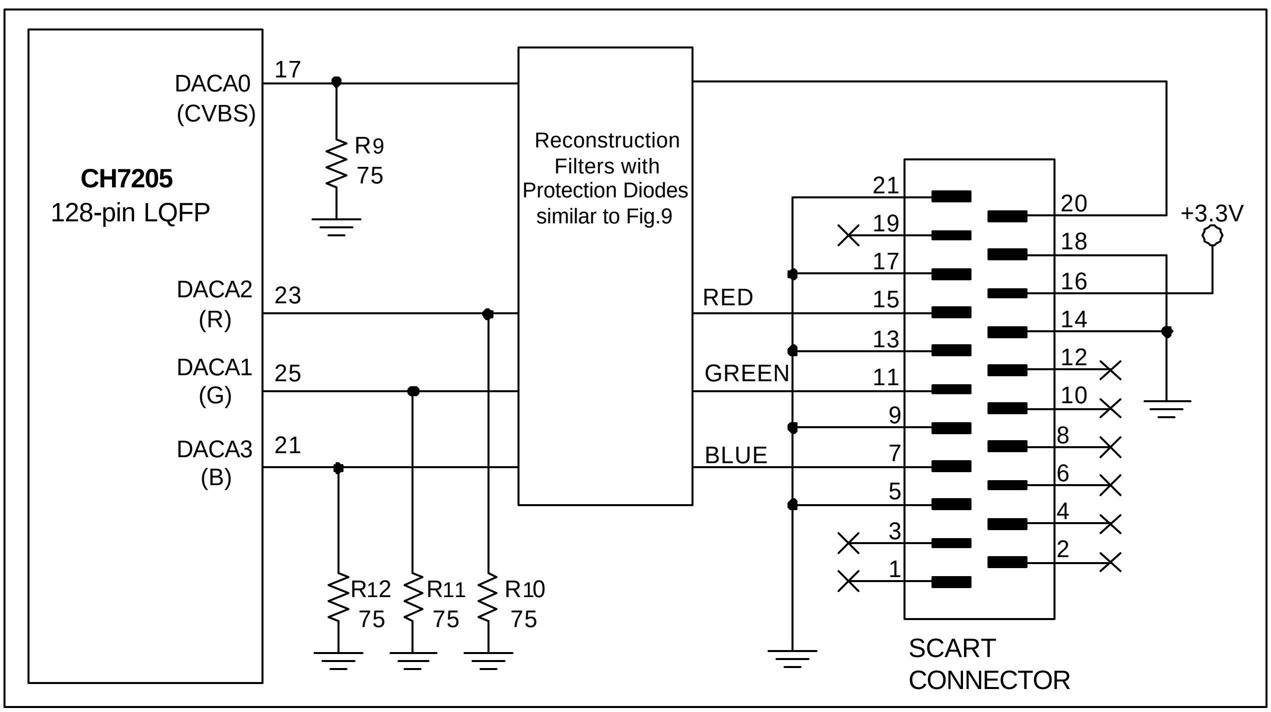


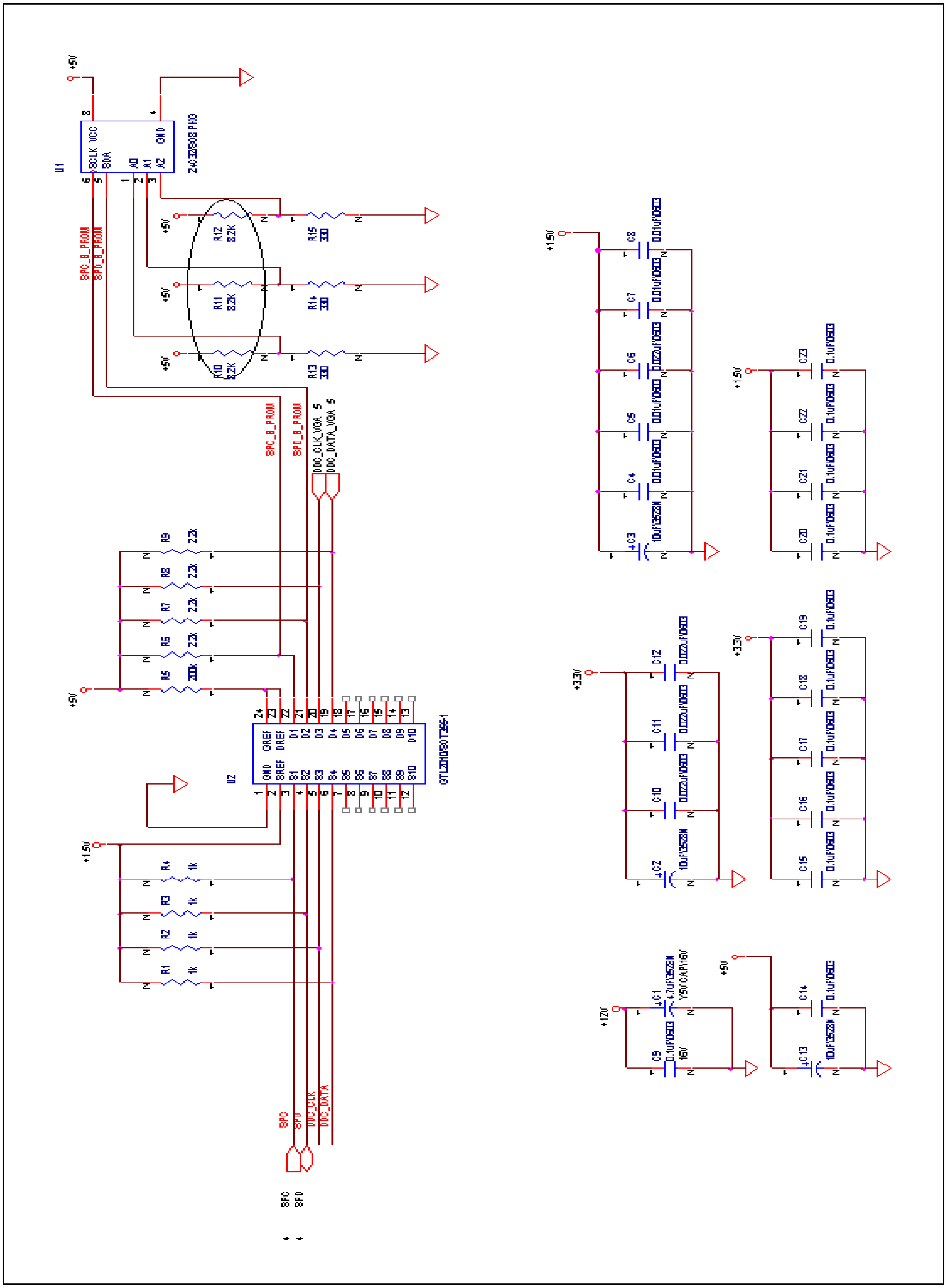

**Figure 13: The Connection for the SCART Connector**

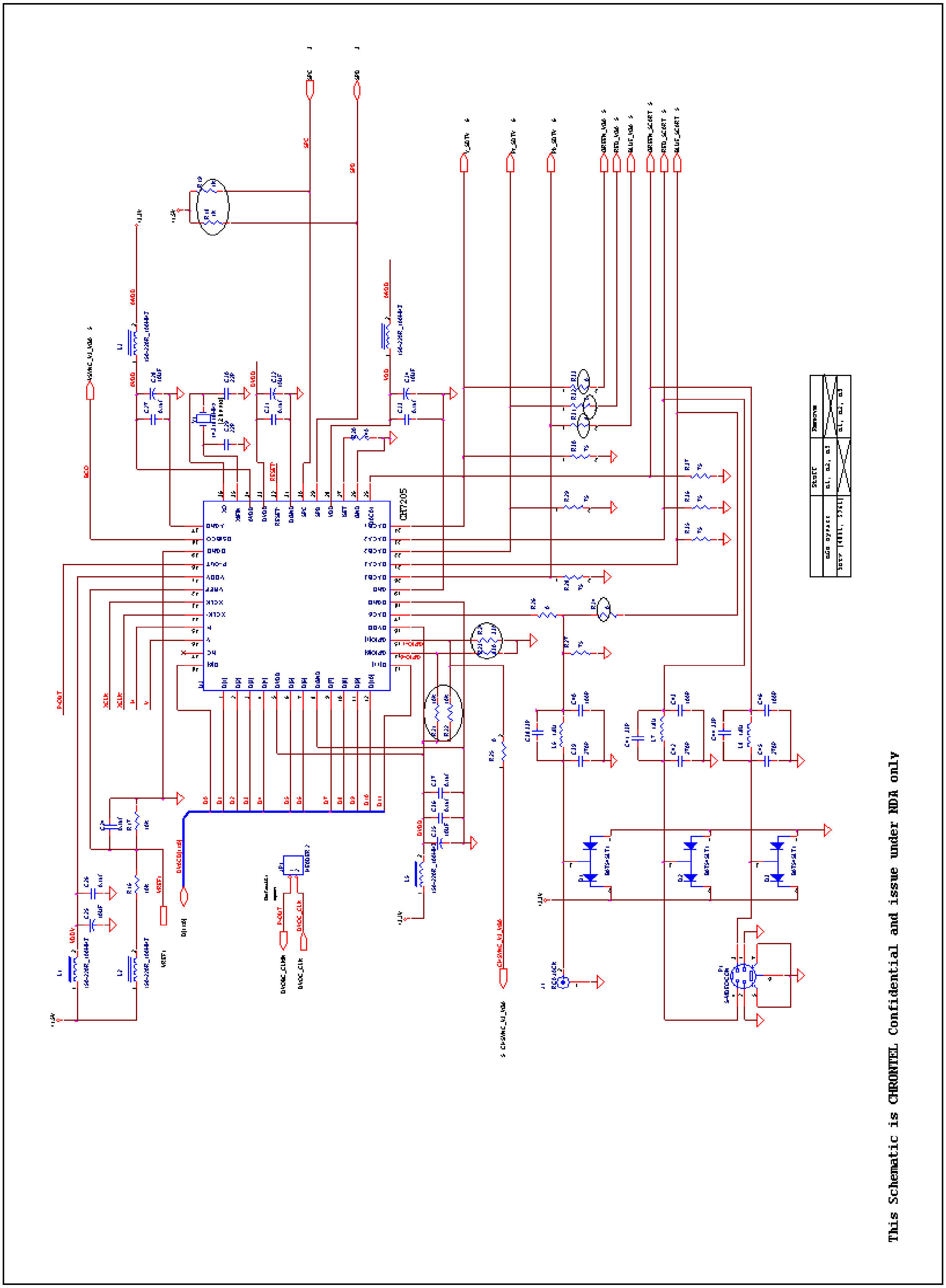
Careful layout consideration for the CVBS, Y and C (or CVBS, R, G and B) traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

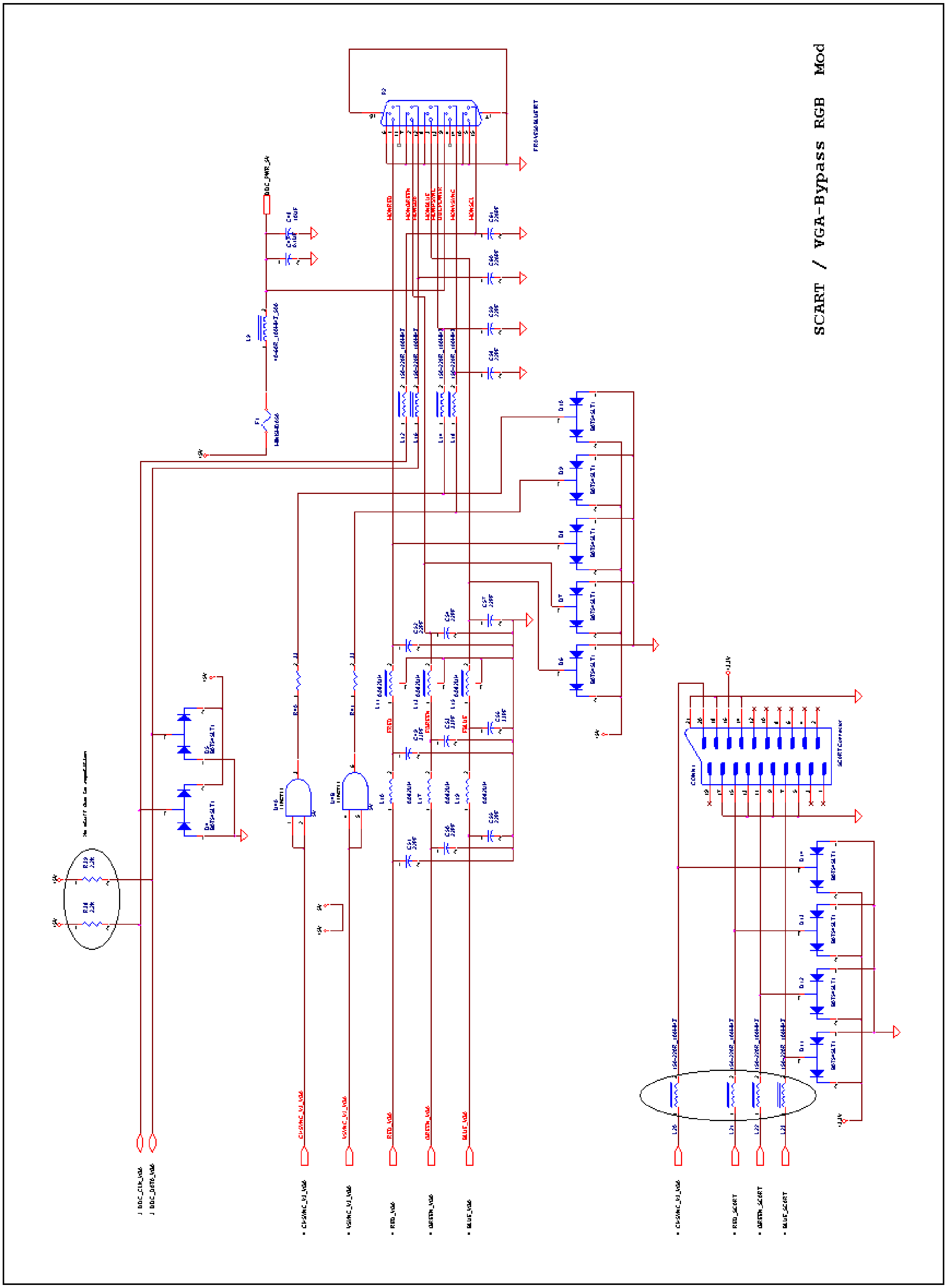
## 3. Reference Design Example

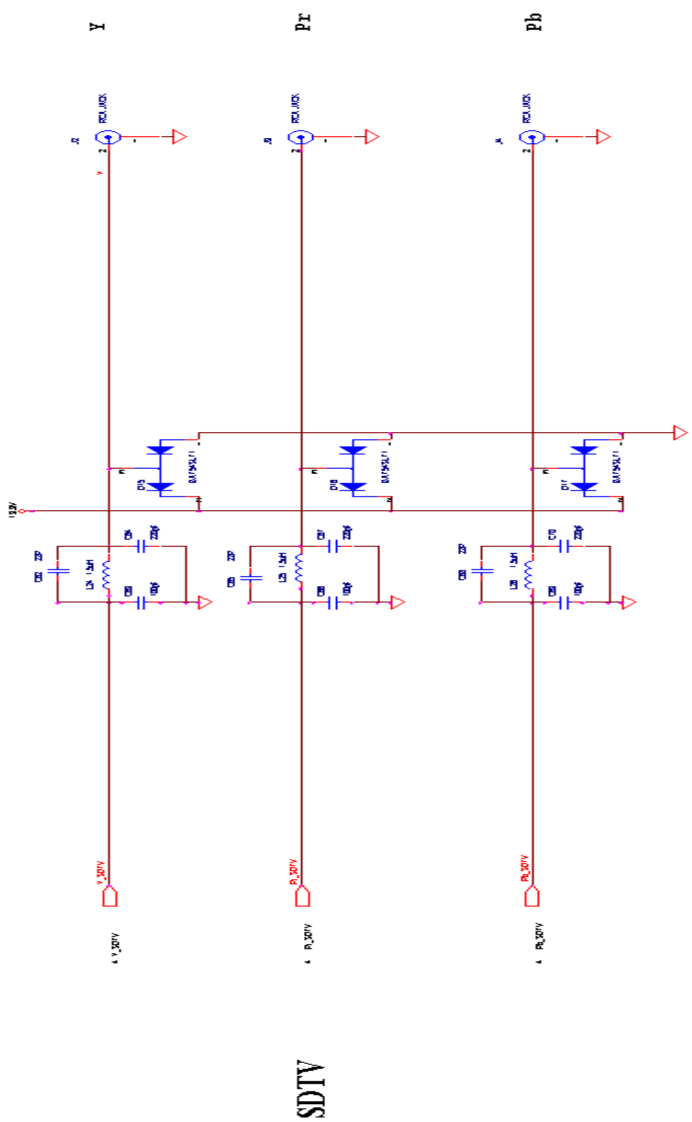
The following schematics are of a CH7205 PCB design used as an example only. It is not a complete design. Those who are seriously doing an application design using the CH7205 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

### 3.1 Schematics of Reference Design Example




CH7205
This Schematic is CHRONTEL Confidential and issue under NDA only


SCART / VGA-Bypass RGB Mod


Y
Pr
Pb
SDTV

## 4. Revision History

| Revision | Date | Section | Description |
|---|---|---|---|
| 1.0 | 5/06/02 | All | First official release, revision 1.0 |
| 1.1 | 8/21/03 | 2.5 | Changed the recommended connections of H (pin 45) and V (pin 46) when in Embedded Sync Mode. A 10K ohm pull down should be connected to the H and V pins when in Embedded Sync Mode. |
| 1.2 | 4/7/04 | 3.1 | Updated reference schematics. |

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Printed in the U.S.A.