

EXPLANATION OF CH7017/CH7019 LVDS POWER SEQUENCING

Description of Problem

When measuring LVDS power sequence timing T1 ~ T5 of CH7017 and CH7019 from a system, it may not correspond exactly to T1 ~ T5 register programming. Furthermore, the waveforms may raise concerns if they are not properly understood. This technical bulletin explains how to measure the LVDS power sequence timing T1 ~ T5 as specified in the Chrontel CH7017 and CH7019 datasheet.

Explanation of the Problem

While T1 ~ T5 can be changed through software, measurements taken from the CH7017 or CH7019 may not always conform to the values programmed through software. Below is the explanation of timing measurements for CH7017/CH7019 LVDS Power Sequencing.

1. T3 timing measurement

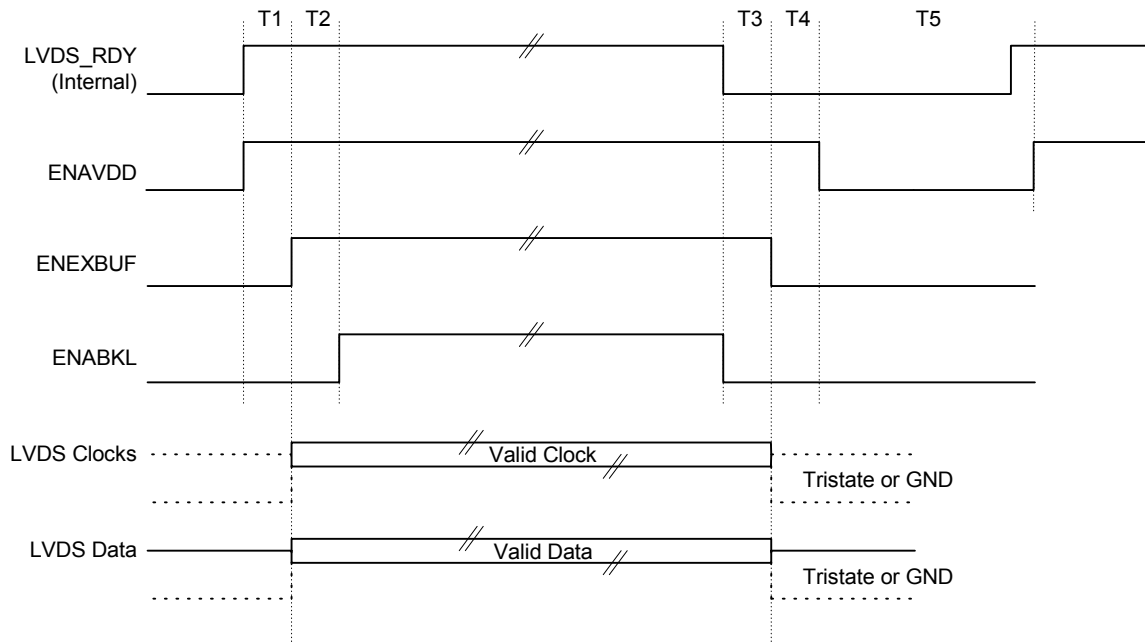


Figure 1: Power sequencing timings

Power sequencing T1 ~ T5 are measured from the waveforms of ENAVDD, ENEXBUF and ENABKL (Refer to **Figure 1**). Because ENEXBUF is an internal signal, the measurement is taken from the LVDS Clock pins instead. LVDS Clocks are controlled by ENEXBUF: If ENEXBUF is off, LVDS Clocks are also off. LVDS Clocks can also be turned off by software. When switching modes, the software may shut down the LVDS Clocks before

ENEXBUF goes low. This creates an error for the measurement on T3. In order to measure T3 correctly, a delay on T3 must be introduced from the software before shutting down the LVDS Clocks. Without this step, T3 will appear to be shorter.

2. T4 timing measurement

T4 timing is measured from the ENAVDD pin. ENAVDD is controlled by an internal state machine within the power sequencing block of the CH7017/CH7019 chip. This state machine is driven by XCLK, which is the external input clock to the CH7017/CH7019 chip. When switching modes, LVDS path and XCLK shuts down, which also stops the state machine that controls ENAVDD. At this time, ENAVDD waveform stays in its current state and T4 cannot be measured. In order to measure T4 correctly, a delay on T4 must be introduced from the software before shutting down the LVDS path. This will ensure that ENAVDD finishes the power down sequence before XCLK stops.

3. A pulse in T5 cycle

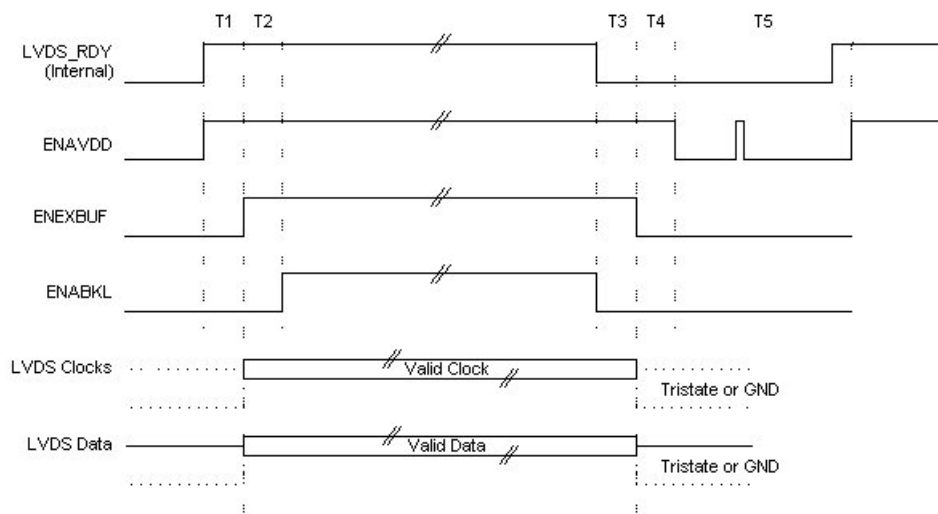


Figure 2: A pulse in T5 cycle

If the incoming signals or some other internal signals are not stable, ENAVDD will not power up. If ENAVDD is already up, but the incoming signals or some other internal signals become unstable, ENAVDD will power down again. This will cause the actual T5 to be longer than what is set in the T5 register, or a pulse in the T5 cycle. This is a protection function of the power sequencing block that has been added as a feature for CH7017 and CH7019.

4. ENAVDD, LVDS Clocks and ENABKL go low together when system powers down

When the system powers down, the device reset bit, RESET* (Pin 58), goes low. As the whole device resets, ENAVDD, LVDS Clocks and ENABKL go low together. Since the power supply also goes low almost at the same time, the LVDS panel will not be damaged.

5. ENAVDD stays high if the display switches from panel to CRT

If T4 register is set within the T4 parameter allowed by VGA for T4, ENAVDD can power down when display switches from panel to CRT, as shown in Figure 3. (Signal 1: ENAVDD; Signal 3: LVDS Clock; Signal 4: XCLK input to CH7017, T4 = 50 ms). Note that the minimum T4 time required for CH7017 or CH7019 is 1ms.

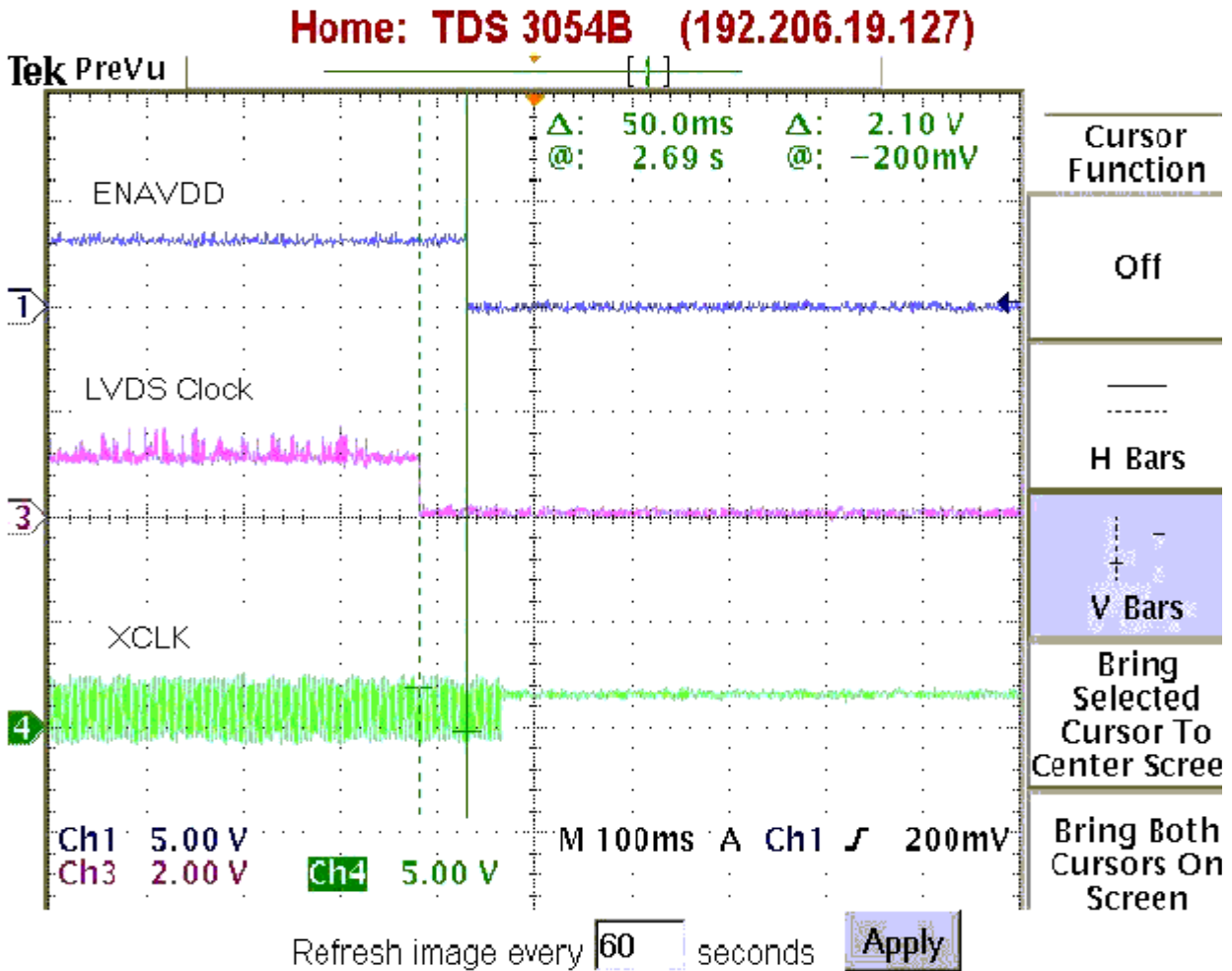


Figure 3: Display switches from panel to CRT (T4=50ms)

If T4 register is set higher than the maximum time allowed by VGA for T4, ENAVDD cannot power down when display switches from panel to CRT, as shown in Figure 4 below. (Signal 1: ENAVDD; Signal 3: LVDS Clock; Signal 4: XCLK input to CH7017, T4 = 100 ms). Note that the maximum T4 time programmable for CH7017 or CH7019 is 512ms.

This is because the state machine in the power sequencing block is triggered by XCLK. If XCLK stops, the state machine also stops running and keeps the current outputs. If T4 is within VGA specified timing, ENAVDD goes low before XCLK stops running. But if T4 exceeds VGA specified timing, ENAVDD cannot finish power down sequence before XCLK stops.

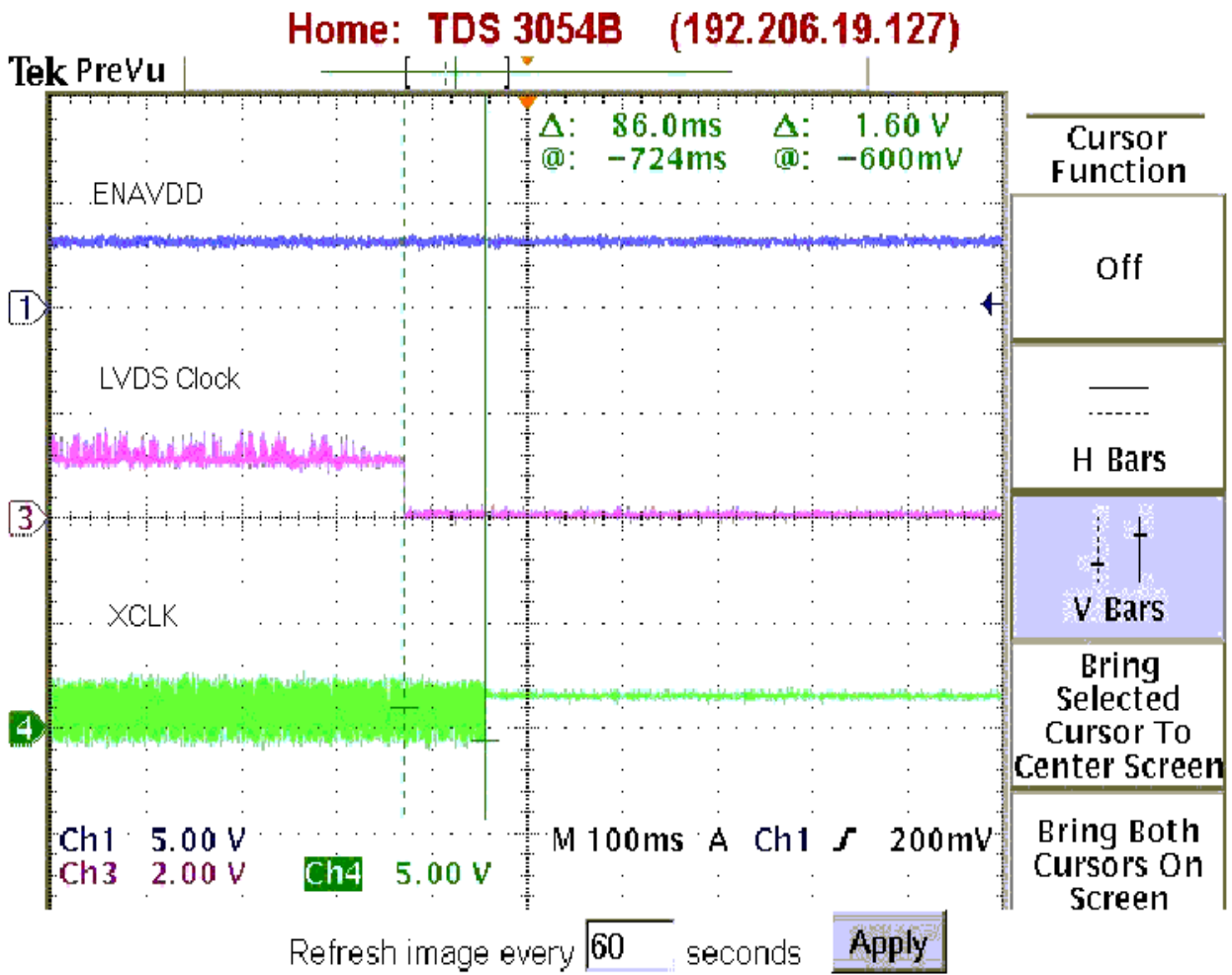


Figure 4: Display switches from panel to CRT (T4=100ms)

Contact Chronitel Applications for assistance on introducing delay for T3 and T4 via software.

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