PCB Layout Considerations for CH7003, CH7004 and CH7013

Introduction

This application note focuses on the basic PCB layout guidelines for the CH7003, CH7004 and CH7013 VGA-to-TV encoder products. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout for these products. These are only recommendations. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 44-pin PLCC package. Users are urged to consult the CH7003/CH7004/CH7013 datasheets for the pin assignments of the corresponding signals in the other packages offered.

Component Placement

Components associated with the CH7003/CH7004/CH7013 encoders should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1 - C6) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7003/CH7004/CH7013 ground pins, in addition to ground vias.

Ground Pins

The analog and digital grounds of the CH7003/CH7004/CH7013 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7003/CH7004/CH7013 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance.

Power Supply Pins

Separate digital, analog, and DAC power planes are recommended. Digital power should be supplied to pins 11, 22, 36, and 44 (DVDD); analog power should be supplied to pin 37 (AVDD); and DAC power should be supplied to pin 31 (VDD). The analog and DAC supplies are connected to a single +5V supply through ferrite beads, as shown in the schematic on **Figure 1**. The digital supplies are powered by either a +5V or a +3.3V supply, depending on the logic level of the input pixel data.

A positive 5V and/or 3.3V regulator may be used if a clean +5V and/or +3.3V supplies are not available. Please refer to **Figures 2** and **3** for the optional positive 5V and 3.3V regulator circuits.

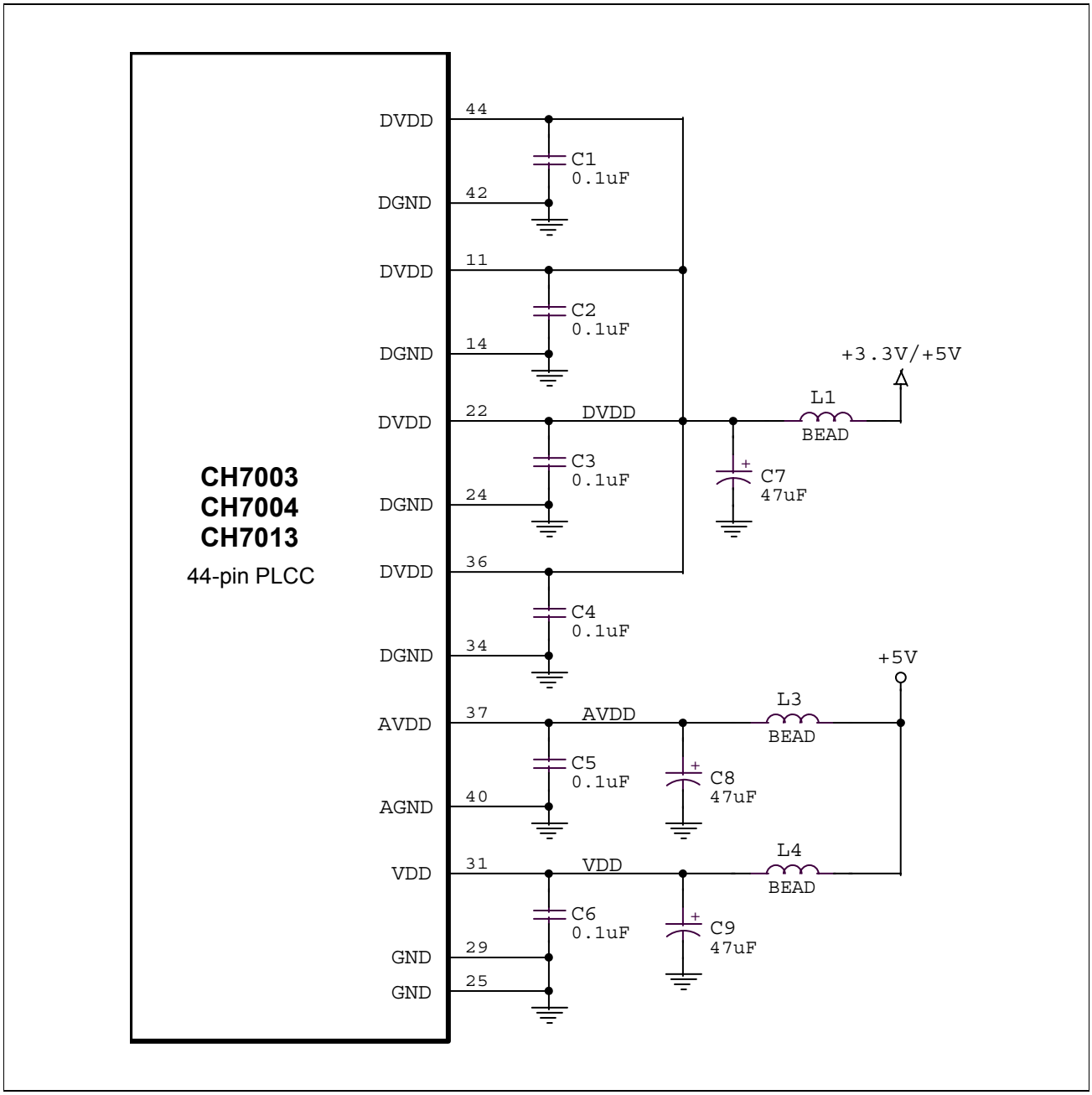

Figure 1: Power Supply Decoupling and Distribution

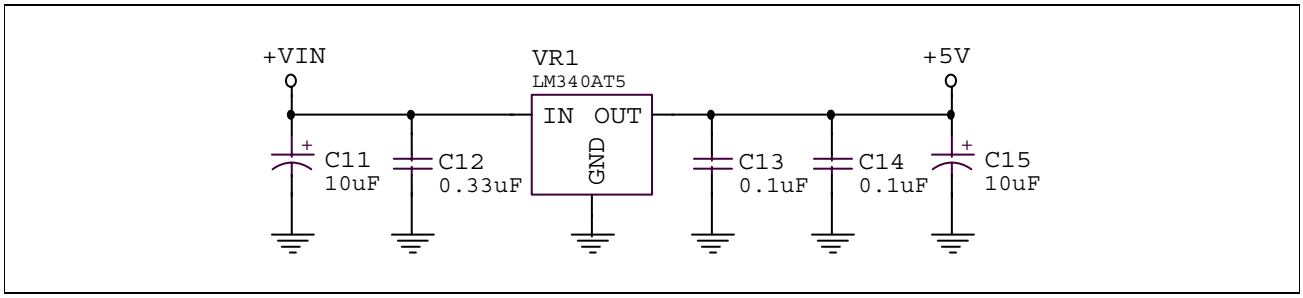

Figure 2: Optional Positive 5V Voltage Regulator

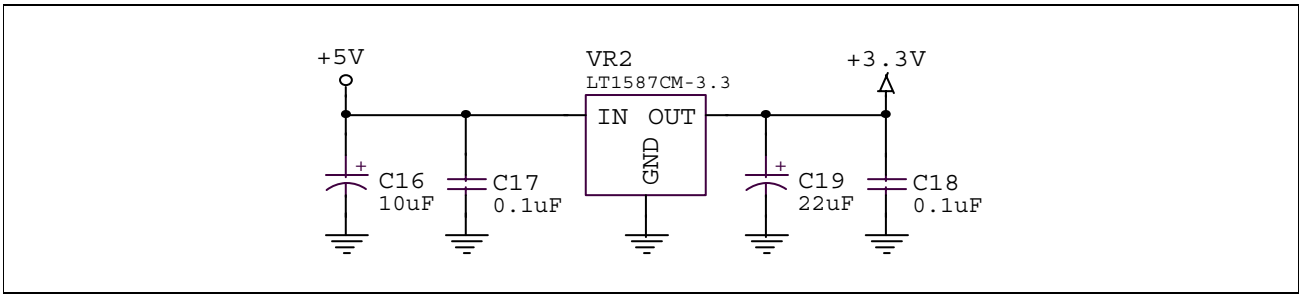

Figure 3: Optional Positive 3.3V Voltage Regulator

RSET pin

A 360Ω RSET resistor should be placed directly and as close as possible to pin 30 with short and wide traces. Whenever possible, the RSET resistor's ground pin should also be connected to the DAC ground pin (pin 29). Otherwise, the ground reference of the RSET resistor should ideally be close to the CH7003/CH7004/CH7013.

Horizontal and Vertical Sync Signals

In input modes where the horizontal and vertical sync signals from the graphics controller are shared between the CH7003/CH7004/CH7013 and the computer monitor, buffering the sync signals prior to connecting them to the monitor is recommended (please refer to **Figure 4** below). These buffers help isolate any noise generated from the monitor connection (e.g., reflections, etc.) from coupling into the sync inputs of the CH7003/CH7004/CH7013, thereby degrading the display quality. In modes where the embedded syncs are used, these buffers are not necessary.

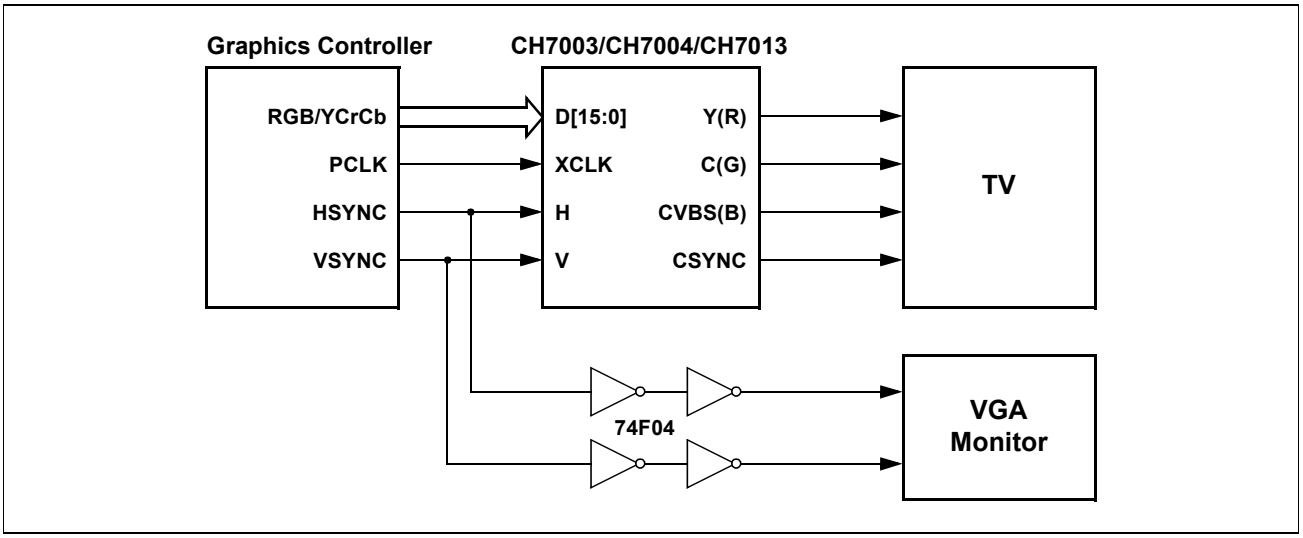

Figure 4: Sync Buffers

Video Inputs

Since the digital pixel data and the pixel clock of the CH7003/CH7004/CH7013 may toggle at speeds up to 100MHz (depending on input mode), it is critical that the connection of these signals between the graphics controller and the CH7003/CH7004/CH7013 be kept short and as isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. Damping each line with a series resistor (30Ω-300Ω) will help minimize ringing on these lines.

Video Outputs

The components associated with the video output pins should be placed as close as possible to the CH7003/CH7004/CH7013. The 75Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7003/CH7004/CH7013 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk.

The output of the CH7003/CH7004/CH7013 may be configured for the following video output types: s-video, composite, and SCART. **Figure 5** illustrates the typical connection for the s-video and composite outputs, while **Figure 6** and **Figure 7** illustrate the connection for the SCART connector.

Please beware that in order to minimize the hazard of ESD, a set of protection diodes MUST BE used for each DAC connecting to TV (Refer to AN-38 for details).

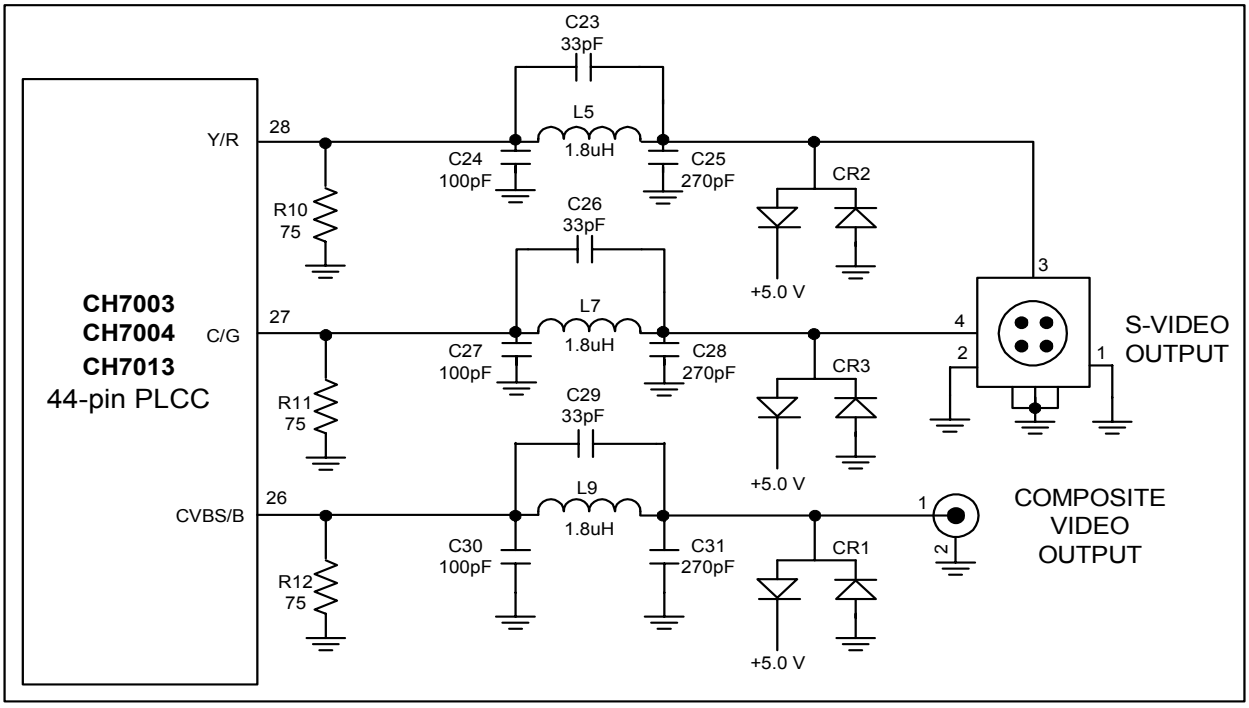

Figure 5: S-Video and Composite Video Outputs

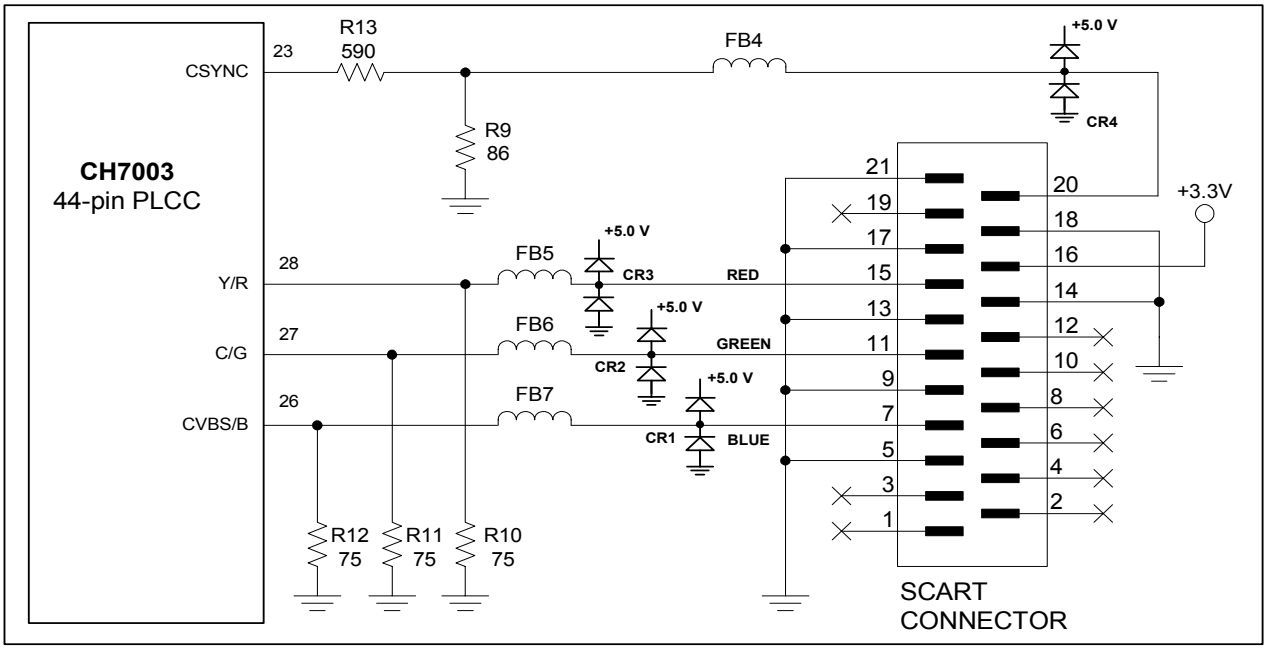

Figure 6: SCART type I Video Output (CH7003)

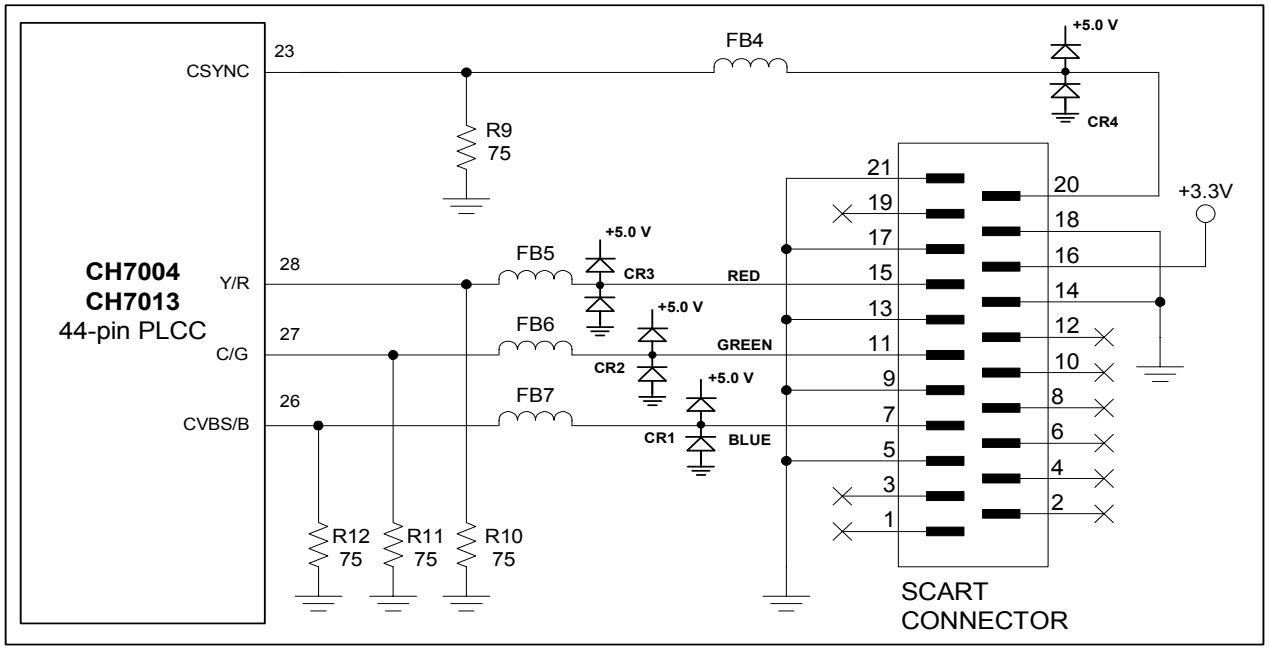

Figure 7: SCART type I Video Output (CH7004/CH7013)

Crystal Input

The 14.31818 MHz (±50ppm) crystal must be placed as close as possible to the XI and XO/FIN pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7003/CH7004/CH7013 encoders, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7003/CH7004/CH7013.

Reference Crystal Oscillator

The CH7003/CH7004/CH7013 includes an oscillator circuit which allows an inexpensive 14.31818 MHz crystal to be connected directly. Alternatively, an externally generated 14.31818 MHz clock source may be supplied to the CH7003/CH7004/CH7013. If an external clock source is used, it should have TTL level specifications. The clock should be connected to the XO/FIN pin, and the XI pin should be tied to ground. The external source must exhibit ±50 ppm or better frequency tolerance, and possess low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

- Crystal is specified as 14.31818 MHz, ±50 ppm in parallel resonance (NOT series resonance).
- Crystal is operated with a load capacitance equal to its specified value.
- External load capacitors have their ground connection very close to the CH7003/CH7004/CH7013.
- To allow tunability, a variable cap may be used from XI to ground.

Note that the XI and XO/FIN pin each have approximately 15-10 pF of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO/FIN pins, the following calculation should be used:

$$\mathbf{Cext} = (\mathbf{2} \times \mathbf{Cload}) - \mathbf{Cint}$$

where: **Cext** = external load capacitance required on XI and XO/FIN pins.

Cload = crystal load capacitance specified by crystal manufacturer

Cint = capacitance internal to CH7003/CH7004/CH7013 (approximately 10-15 pF on each of XI and XO/FIN pins)

Note: External load capacitance shall include routing capacitance on the PCB.

Please refer to **Figure 8** for the symbols used in the calculation described above.

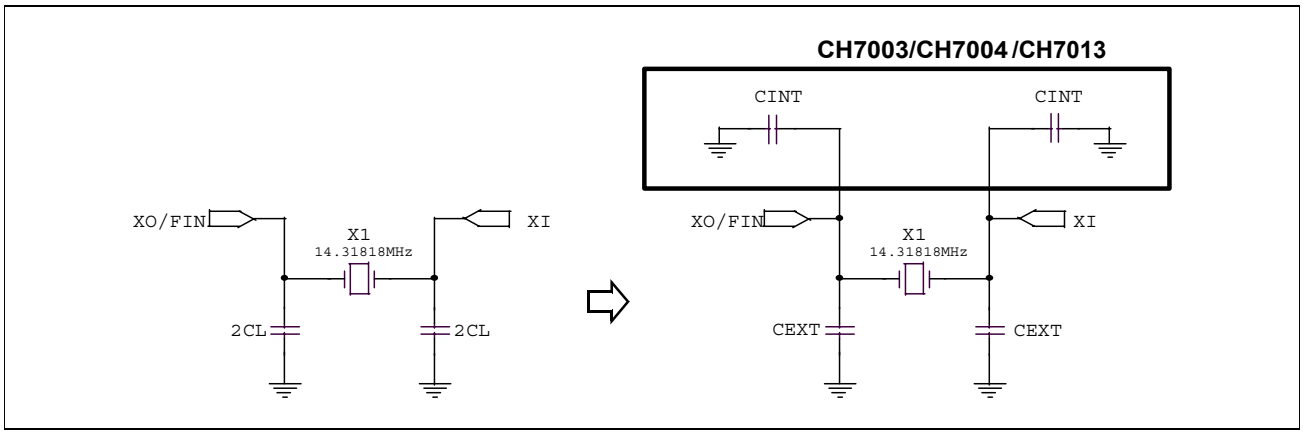

Figure 8: Reference Crystal