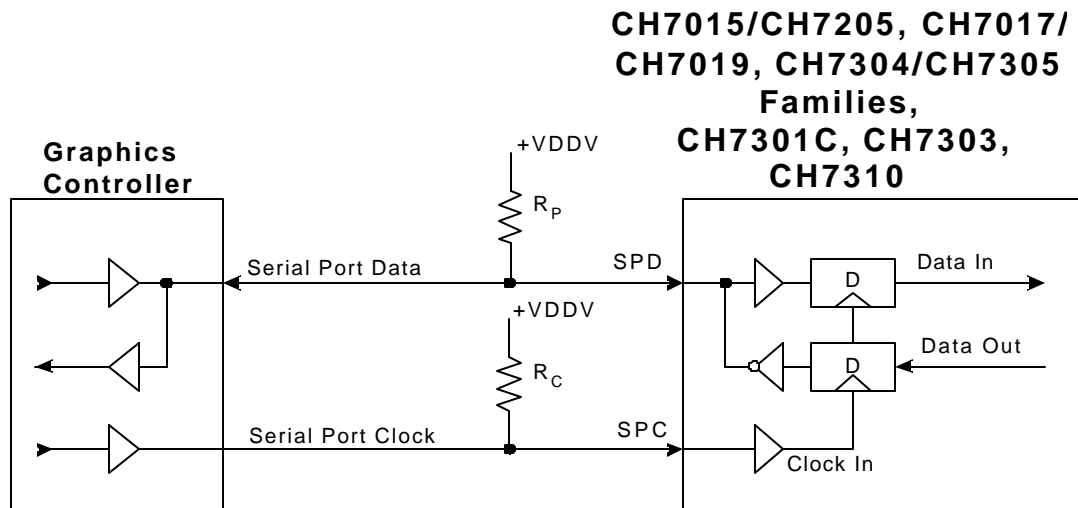


**CH7015/CH7205, CH7017/CH7019, CH7304/CH7305 Families, CH7301C and CH7303/CH7310 Registers Read/Write Operation**

**1. Introduction**

The Chrontel CH7015/CH7205, CH7017/CH7019, CH7304/CH7305 families and the CH7301C/CH7303/CH7310 all contain a serial port interface, through which the control registers can be written to and read from. The serial interface consists of SPD (bidirectional serial port data) and SPC (serial port clock).

The serial port clock line (SPC) is input only and is driven by the output buffer of the graphics controller device, which is the clock master in the system. The serial port data line (SPD) is either input to or output from the encoder depending on the write or read status. The data on the line can be transferred up to 400 kbits/s. **Figure 1** shows the connection of the serial port interface.



**Figure 1: The Connection of the Serial Port Interface.**

## 2. Serial Port Operation

### 2.1 Electrical Characteristics of the Serial Port

The connections of the serial port interface is shown in **Figure 1**. A pull-up resistor ( $R_p$ ) must be connected to the same voltage supply seen by the serial port interface pins. The serial port input voltage level is determined by  $V_{DDV}$  (1.1V - 3.3V).

A weak pull-up resistor ( $R_C$ ) may be added to the clock line to ensure that it is pulled high when the line is free.

#### Maximum and minimum values of pull-up resistor ( $R_p$ )

The value of  $R_p$  depends on the following parameters:

- Supply voltage
- Line capacitance
- Number of devices connected (input current + leakage current =  $I_{input}$ )

The supply voltage limits the minimum value of resistor  $R_p$  due to the specified minimum sink current of 2mA at  $V_{OL_{max}} = 0.4$  V for the output stages:

$$R_p \geq (V_{DD} - 0.4) / 2 \quad (R_p \text{ in } k\Omega)$$

The line capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of  $R_p$  due to the specified rise time. The equation for  $R_p$  is shown below:

$$R_p \leq 10^3 / C \quad (\text{where: } R_p \text{ is in } k\Omega \text{ and } C, \text{ the total capacitance, is in pF})$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10  $\mu$ A. Due to the desired noise margin of  $0.2V_{DD}$  for the HIGH level, the input current limits the maximum value of  $R_p$ . The  $R_p$  limit depends on  $V_{DD}$  and is shown below:

$$R_p \leq (100 \times V_{DD}) / I_{input} \quad (\text{where: } R_p \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A)$$

### 2.2 Transfer Protocol

Both read and write cycles can be executed in “Auto-increment”, “Single-step”, or “Alternating modes”. Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access so that the next register address does not need to be resent through the SPC/SPD serial interface lines. When Auto-increment is set, the initial address is first sent to the encoder then data1 is sent, then data2, then data3, and so forth. Single-step mode, is a simplified version of the Auto-increment mode with a single set of data instead of multiple data that is sent to or received from a specific register. In Alternating mode, a register address is expected prior to each read or write transfer (i.e., transfers alternate between address and data). A basic serial port transfer protocol is shown in **Figure 2**.

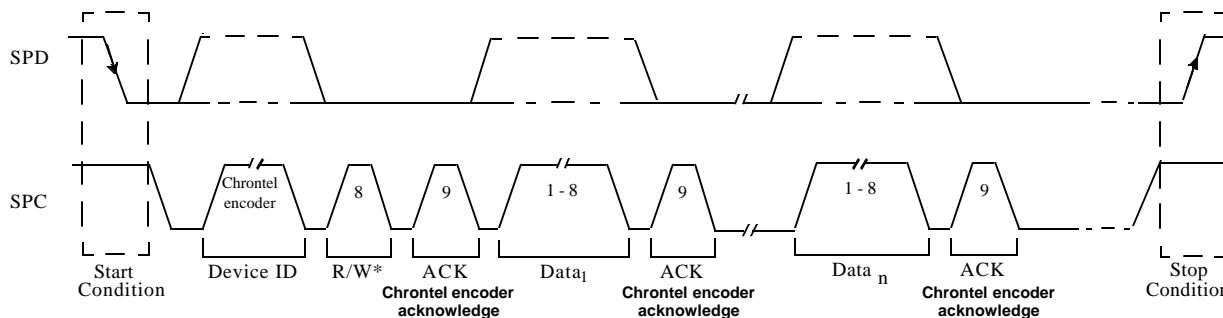


Figure 2: Serial Port Transfer Protocol

The description of the transfer protocol is as follows:

The transfer sequence is initiated when a high-to-low transition of SPD occurs while SPC is high; this is the “START” condition. Transitions of address and data bits can only occur while SPC is low.

The transfer sequence is terminated when a low-to-high transition of SPD occurs while SPC is high; this is the “STOP” condition.

Upon receiving the first START condition, the Chrontel encoder expects a Device Address Byte (DAB) from the master device. The DAB data format is shown below. Bits B[7:1] of the DAB is referred to as the serial port address. When the AS pin of the CH7017/CH7019/CH7301C/CH7303/CH7310 is pulled high, the Device Address Byte becomes ECh for serial port writes and EDh for serial port reads. When the AS pin of the CH7017/CH7019/CH7301C/CH7303/CH7310 is pulled low, the Device Address Byte becomes EAh for serial port writes and EBh for serial port reads. The CH7015/CH7205, CH7304, and CH7305 on the other hand does not have an external AS pin. For the CH7015, CH7304, and CH7305, the AS bit is internally strapped high and for the CH7205, the AS bit is internally strapped low. The Device Address Byte for the CH7015, CH7304, and CH7305 is EAh for serial port writes and EBh for serial port reads. For the CH7205, the Device Address Byte is ECh for serial port writes and EDh for serial port reads.

After the DAB is received, the Chrontel encoder expects a Register Address Byte (RAB) from the master. The data format of the RAB is shown below.

**Device Address Byte (DAB)**

**CH7017A / CH7019A / CH7019B / CH7301C / CH7303 DAB**

| B7 | B6 | B5 | B4 | B3 | B2  | B1 | B0  |
|----|----|----|----|----|-----|----|-----|
| 1  | 1  | 1  | 0  | 1  | AS* | AS | R/W |

**CH7015 / CH7304 / CH7305 DAB (AS bit strapped high)**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0  |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 1  | 0  | 1  | 0  | 1  | R/W |

**CH7205 DAB (AS bit strapped low)**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0  |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 1  | 0  | 1  | 1  | 0  | R/W |

**AS Address Select**

For the CH7017/CH7019, CH7301C and the CH7303/CH7310, the value of this bit is determined by the status of the AS pin. When the pin is strapped high, the value of AS = 1. When the pin is strapped low, the value of AS = 0. The CH7015/CH7205, CH7304 and CH7305 do not have and external AS pin.

**R/W Read/Write Indicator**

- “0”: The master device will write to the encoder at the register location specified by the address AR[6:0]
- “1”: The master device will read from the encoder at the register location specified by the address AR[6:0].

**Register Address Byte (RAB)**

|         |       |       |       |       |       |       |       |
|---------|-------|-------|-------|-------|-------|-------|-------|
| B7      | B6    | B5    | B4    | B3    | B2    | B1    | B0    |
| AutoInc | AR[6] | AR[5] | AR[4] | AR[3] | AR[2] | AR[1] | AR[0] |

**AutoInc Register Address Auto-Increment - used to facilitate sequential R/W of registers**

“1”: Auto-Increment enabled (Auto-increment and Single-step modes).

Write: After the data has been written into the register, the Address Register will automatically increment by one.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will automatically be incremented by one. However, for the first read after an RAB, the Address Register will remain unchanged.

“0”: Auto-Increment disabled (Alternating mode).

Write: After the data has been written into the register, the Address Register will remain unchanged until a new RAB is written.

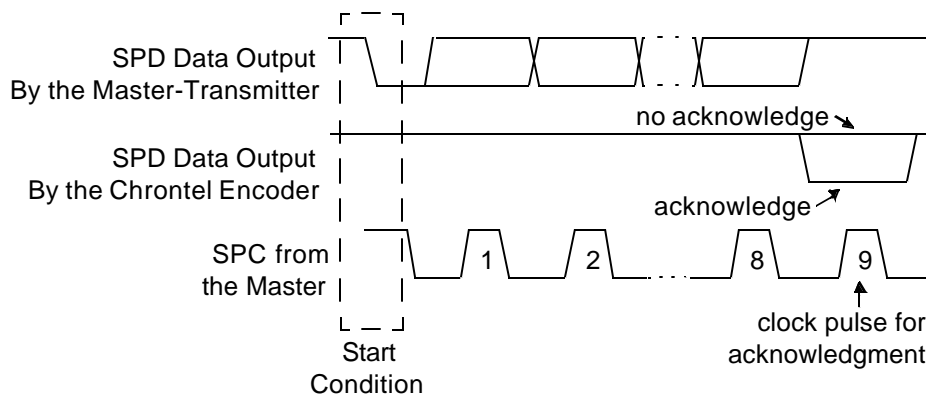
Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will remain unchanged.

**AR[6:0] Register Address - Specifies the Address of the Register to be Accessed**

The value of AR[6:0] will be loaded into the Address Register of the Chronitel encoder. The R/W access, which follows, will be directed to the register specified by Address Register.

**2.3 Chronitel Encoder Write Cycle Protocol (R/W = 0)**

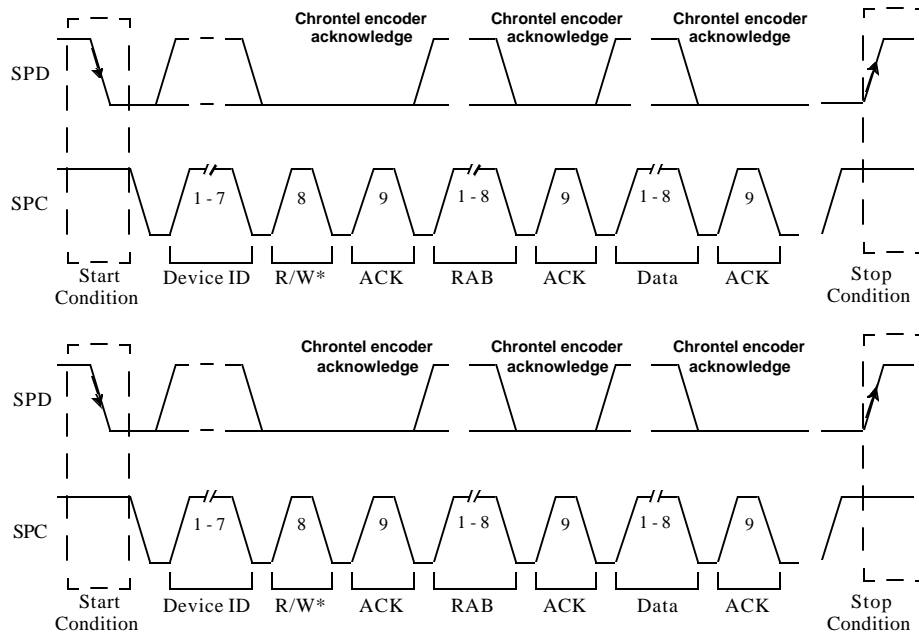
An acknowledge is required for all data transfers. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SPD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SPD line, during the acknowledge clock pulse, so that it remains LOW during the HIGH period of the clock pulse. Note that the resultant state of SPD is the wired-AND of data outputs from the transmitter and receiver. **Figure 3** shows the acknowledge protocol.



**Figure 3: Acknowledge Protocol**

• **Auto-increment / Single-step modes (AutoInc = 1)**

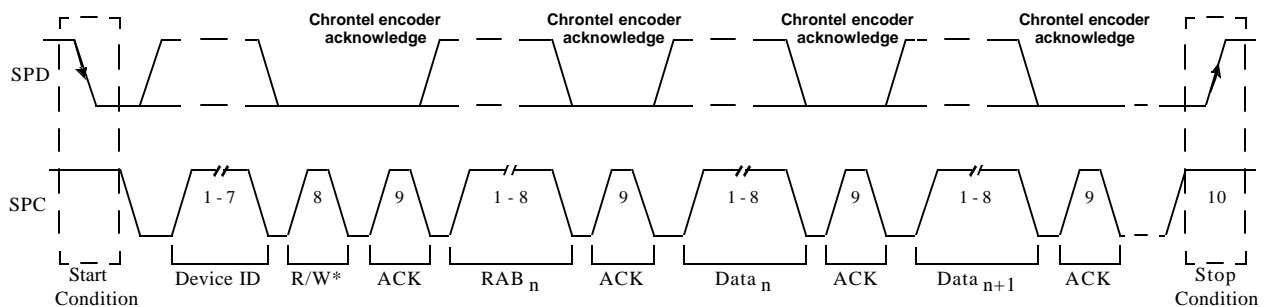
**Figure 4** represents two consecutive Single step write cycles. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[6:0]. The serial interface bus will then enter the “Stop Condition” immediately after the acknowledge has been received. The cycle is then repeated for each subsequent write cycle.



**Note:** The acknowledge is from the Chrontel encoder (slave).

**Figure 4: Single-step Write Cycles (2 cycles)**

An Auto-increment write cycle is shown in **Figure 5**. During the Auto-increment mode transfers, the register address pointer continues to increment for each data write cycle until AR[6:0] = the last accessible Address Register of the encoder. The next byte of information represents a new auto-sequencing “Starting address”, which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new “Starting address”. The Auto-increment sequence can be terminated any time by either a “STOP” or “RESTART” condition. The write operation can be terminated with a “STOP” condition.



**Figure 5: Auto-Increment Write Cycle**

**Notes:** The acknowledge is from the Chrontel encoder (slave).

• **Alternating mode (AutoInc = 0)**

Figure 6 shows two consecutive alternating write cycles (AutoInc = 0 and R/W = 0). The byte following the Register Address Byte (RAB), is the data to be written into the register specified by AR [6:0]. And then another RAB is expected from the master device, followed by another data byte, and so on

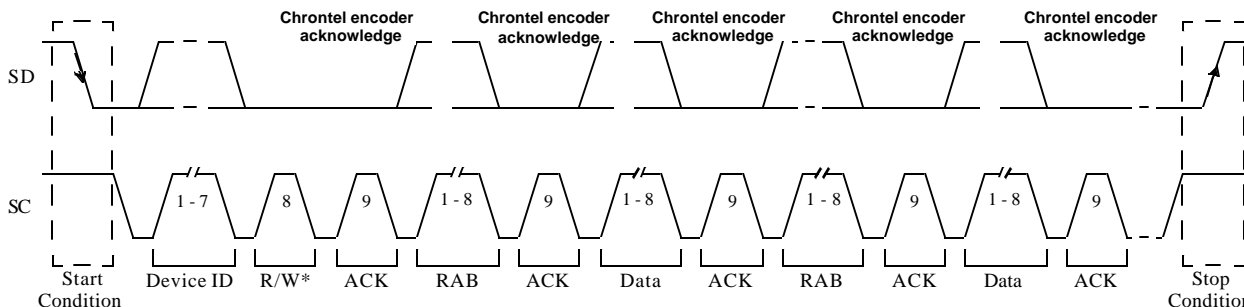


Figure 6: Alternating Write Cycles

Notes: The acknowledge is from the Chrontel Encoder.

**2.4 Chrontel Encoder Read Cycle Protocol (R/W = 1)**

The master-receiver must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter encoder will then release the data line to allow the master to generate either the STOP condition or the RESTART condition.

• **Auto-Increment/ Single modes (AutoInc = 1)**

To read the content of the registers, the master device must first issue a “START” condition (or a “RESTART” condition). After the START condition, the first byte of data will be the DAB with R/W = 0. The second byte is the RAB with AR[6:0] containing the address of the register that the master device intends to read from. The master device must then issue a “RESTART” condition (“RESTART” = “START”, without a previous “STOP” condition). The first byte of data, after the RESTART condition, is another DAB with R/W=1, indicating the master’s intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). For Single-step mode, a “Stop” condition or “Restart” condition is sent out immediately after the acknowledge which indicates that the data has been read (see Figure 7).

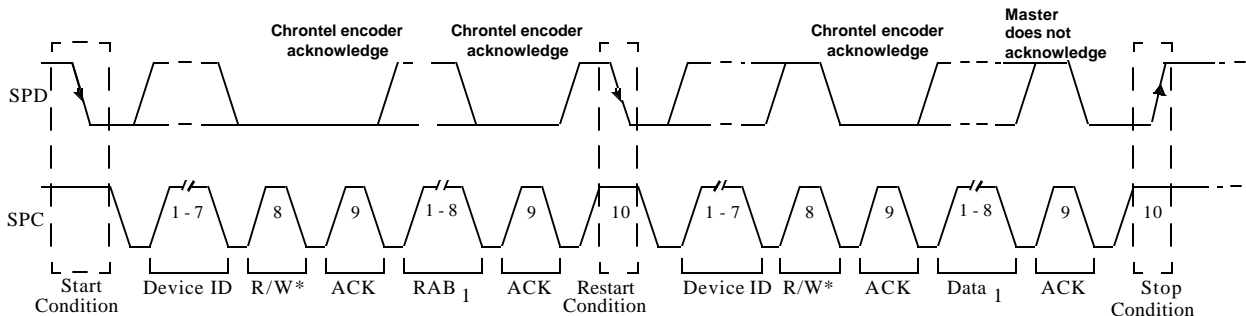
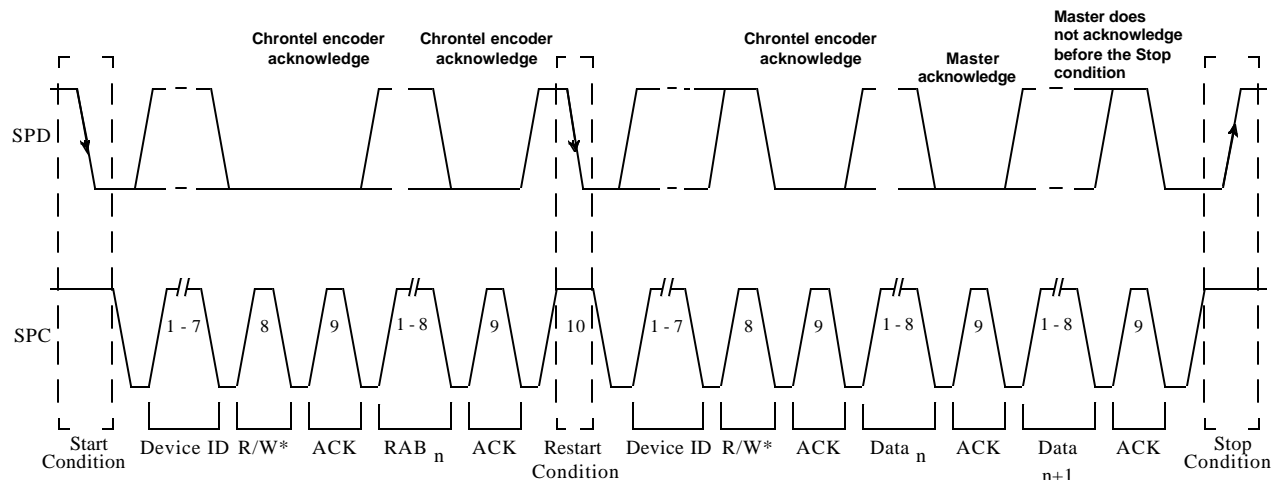


Figure 7: Single-step Read Cycles (2 cycles)

For Auto-increment read cycles, the address register is incremented automatically. This allows subsequent data bytes to be read from successive registers without having to provide a second RAB.

Regarding the Auto-increment read cycle, the address register continues to increment for each read cycle. When AR[6:0] of the RAB has been incremented to the last accessible register address of the encoder, the Address Register will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 8** shows an Auto-increment read cycle terminated by a STOP condition.



**Figure 8: Auto-increment Read Cycles**

- **Alternating mode (AutoInc = 0)**

In Alternating mode, another RESTART condition, followed by another DAB with R/W = 0 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. After that, the master may read another data byte, and so on. In summary, a RESTART condition, followed by a DAB, must be produced by the master before each of the RAB, and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 9**.

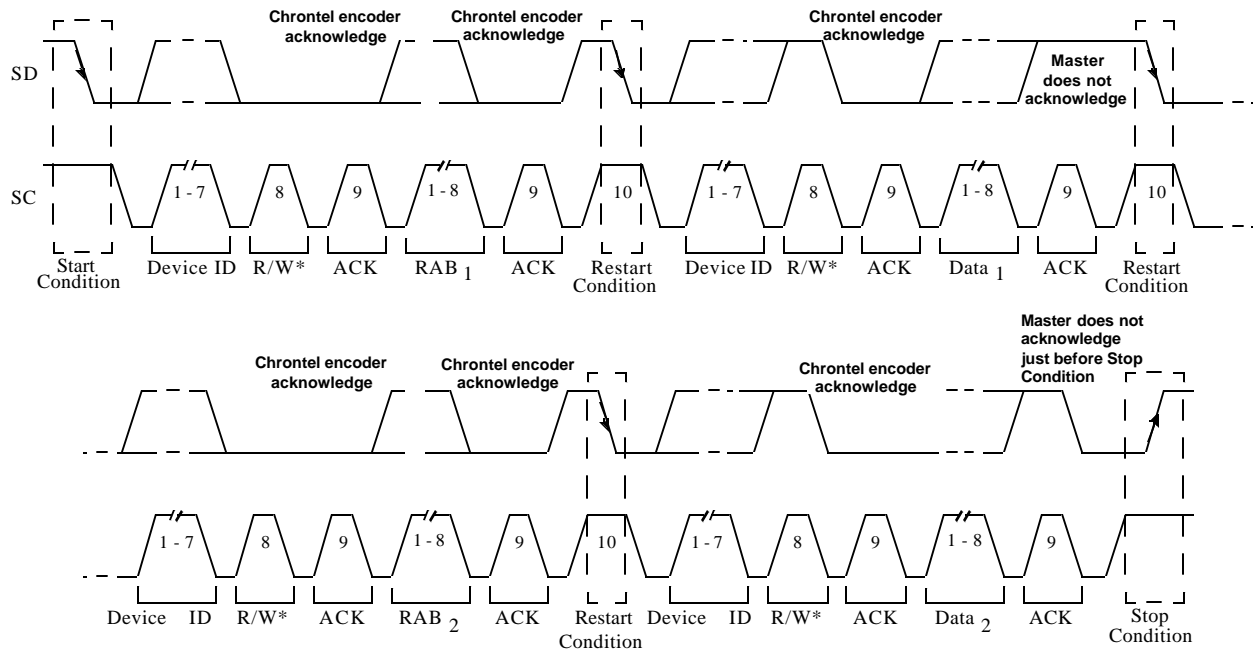


Figure 9: Alternating Read Cycles

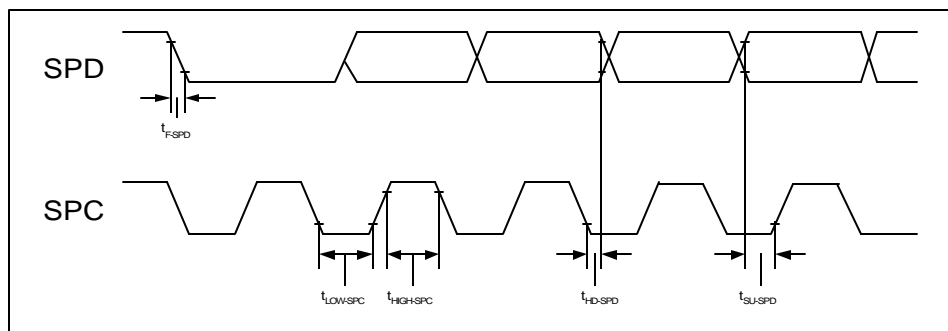
### 3. Electrical Specifications

**Table 1: DC Specifications**

| Symbol     | Description                               | Test Condition            | Min     | Typ | Max             | Unit |
|------------|---|---------------------------|---------|-----|-----------------|------|
| $V_{SDOL}$ | SPD (serial port data) Output Low Voltage | $I_{OL} = 2.0 \text{ mA}$ |         |     | 0.4             | V    |
| $V_{SPIH}$ | Serial Port (SPC, SPD) Input High Voltage |                           | 1.0     |     | $V_{DDV} + 0.5$ | V    |
| $V_{SPIL}$ | Serial Port (SPC, SPD) Input Low Voltage  |                           | GND-0.5 |     | 0.4             | V    |

**Table 2: AC Specifications**

| Symbol         | Description              | Test Condition | Min | Typ | Max | Unit          |
|----------------|--------------------------|----------------|-----|-----|-----|---------------|
| $f_{SPC}$      | SPC clock frequency      |                | 0   |     | 400 | kHz           |
| $t_{LOW-SPC}$  | Low Period of SPC clock  |                | 1.3 |     |     | $\mu\text{s}$ |
| $t_{HIGH-SPC}$ | High Period of SPC clock |                | 0.6 |     |     | $\mu\text{s}$ |
| $t_{SU-SPD}$   | Data setup time          |                | 100 |     |     | ns            |
| $t_{HD-SPD}$   | Data hold time           |                | 0   |     |     | ns            |
| $t_{F-SPD}$    | Fall time of SPD signal  | Load = 400pf   |     |     | 300 | ns            |



**Figure 10: Serial Port Interface Timing**

**Appendix: Registers Maps of the CH7015/CH7205, CH7017/CH7019, and CH7304/CH7305 Encoders**

**Table 3: Non-Macrovision registers map of the CH7015**

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00h      | IR2      | IR1      | IR0      | VOS1     | VOS0     | SR2      | SR1      | SR0      |
| 01h      | VOF1     | VOF0     | CFF1     | CFF0     | YFFH1    | YFFH0    | YFFL1    | YFFL0    |
| 02h      | VBID     | CFRB     | CVBWB    | CBW      | YSV1     | YSV0     | YCV1     | YCV0     |
| 03h      | Reserved | Reserved | SAV8     | HP8      | VP8      | TE2      | TE1      | TE0      |
| 04h      | SAV7     | SAV6     | SAV5     | SAV4     | SAV3     | SAV2     | SAV1     | SAV0     |
| 05h      | HP7      | HP6      | HP5      | HP4      | HP3      | HP2      | HP1      | HP0      |
| 06h      | VP7      | VP6      | VP5      | VP4      | VP3      | VP2      | VP1      | VP0      |
| 07h      | BL7      | BL6      | BL5      | BL4      | BL3      | BL2      | BL1      | BL0      |
| 08h      | Reserved | DACS1    | DACS0    | CMPLMT   | MEDFEN   | CE2      | CE1      | CE0      |
| 09h      | MEM2     | MEM1     | MEM0     | N9       | N8       | M8       | PLLCP1   | PLLCP0   |
| 0Ah      | M7       | M6       | M5       | M4       | M3       | M2       | M1       | M0       |
| 0Bh      | N7       | N6       | N5       | N4       | N3       | N2       | N1       | N0       |
| 0Ch      | FSCI31   | FSCI30   | FSCI29   | FSCI28   | FSCI27   | FSCI26   | FSCI25   | FSCI24   |
| 0Dh      | FSCI23   | FSCI22   | FSCI21   | FSCI20   | FSCI19   | FSCI18   | FSCI17   | FSCI16   |
| 0Eh      | FSCI15   | FSCI14   | FSCI13   | FSCI12   | FSCI11   | FSCI10   | FSCI9    | FSCI8    |
| 0Fh      | FSCI7    | FSCI6    | FSCI5    | FSCI4    | FSCI3    | FSCI2    | FSCI1    | FSCI0    |
| 10h      | SICP     | SICN     | CIV25    | CIV24    | CIVC1    | CIVC0    | PALN     | CIVEN    |
| 11h      | CIV23    | CIV22    | CIV21    | CIV20    | CIV19    | CIV18    | CIV17    | CIV16    |
| 12h      | CIV15    | CIV14    | CIV13    | CIV12    | CIV11    | CIV10    | CIV9     | CIV8     |
| 13h      | CIV7     | CIV6     | CIV5     | CIV4     | CIV3     | CIV2     | CIV1     | CIV0     |
| 14h      | BGBST    | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HDTV     |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | M/S*     | MCP      | PCM      | XCM      |
| 1Dh      | Reserved | BLKEN    | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | GOENB1   | GOENB0   | GPIOL1   | GPIOL0   | Reserved | Reserved | POUTE    | POUTP    |
| 1Fh      | IBS      | DES      | SYO      | VSP      | HSP      | IDF2     | IDF1     | IDF0     |
| 20h      | Reserved | XOSC2    | Reserved | DACT3    | DACT2    | DACT1    | DACT0    | SENSE    |
| 21h      | XOSC1    | XOSC0    | Reserved | SYNCO1   | SYNCO0   | DACG1    | DACG0    | DACBP    |
| 22h      | SHF2     | SHF1     | SHF0     | BCOEN    | BCOP     | BCO2     | BCO1     | BCO0     |
| 48h      | GPHSS    | VSGLN    | Reserved | ResetIB  | ResetDB  | Reserved | Reserved | Reserved |
| 49h      | Reserved | Reserved | Reserved | DACPD3   | DACPD2   | DACPD1   | DACPD0   | TVPD     |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 4Ch      | WSSD7    | WSSD6    | WSSD5    | WSSD4    | WSSD3    | WSSD2    | WSSD1    | WSSD0    |
| 4Dh      | WSSD15   | WSSD14   | WSSD13   | WSSD12   | WSSD11   | WSSD10   | WSSD9    | WSSD8    |
| 4Eh      | WSSEN    | WSSUVF   | WSSS1    | WSSS0    | WSSD19   | WSSD18   | WSSD17   | WSSD16   |
| 4Fh      | PEDL7    | PEDL6    | PEDL5    | PEDL4    | PEDL3    | PEDL2    | PEDL1    | PEDL0    |
| 55h      | IQEN     | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Table 4: Non-Macrovision registers map of the CH7205

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00h      | IR2      | IR1      | IR0      | VOS1     | VOS0     | Reserved | Reserved | Reserved |
| 01h      | VOF1     | VOF0     | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 02h      | VBID     | CFRB     | CVBWB    | CBW      | YSV1     | YSV0     | YCV1     | YCV0     |
| 03h      | Reserved | Reserved | SAV8     | HP8      | VP8      | Reserved | Reserved | Reserved |
| 04h      | SAV7     | SAV6     | SAV5     | SAV4     | SAV3     | SAV2     | SAV1     | SAV0     |
| 05h      | HP7      | HP6      | HP5      | HP4      | HP3      | HP2      | HP1      | HP0      |
| 06h      | VP7      | VP6      | VP5      | VP4      | VP3      | VP2      | VP1      | VP0      |
| 07h      | BL7      | BL6      | BL5      | BL4      | BL3      | BL2      | BL1      | BL0      |
| 08h      | Reserved | Reserved | Reserved | Reserved | Reserved | CE2      | CE1      | CE0      |
| 09h      | MEM2     | MEM1     | MEM0     | N9       | N8       | M8       | PLLCPI   | PLLCAP   |
| 0Ah      | M7       | M6       | M5       | M4       | M3       | M2       | M1       | M0       |
| 0Bh      | N7       | N6       | N5       | N4       | N3       | N2       | N1       | N0       |
| 0Ch      | FSCI31   | FSCI30   | FSCI29   | FSCI28   | FSCI27   | FSCI26   | FSCI25   | FSCI24   |
| 0Dh      | FSCI23   | FSCI22   | FSCI21   | FSCI20   | FSCI19   | FSCI18   | FSCI17   | FSCI16   |
| 0Eh      | FSCI15   | FSCI14   | FSCI13   | FSCI12   | FSCI11   | FSCI10   | FSCI9    | FSCI8    |
| 0Fh      | FSCI7    | FSCI6    | FSCI5    | FSCI4    | FSCI3    | FSCI2    | FSCI1    | FSCI0    |
| 10h      | SICP     | SICN     | CIV25    | CIV24    | CIVC1    | CIVC0    | PALN     | CIVEN    |
| 11h      | CIV23    | CIV22    | CIV21    | CIV20    | CIV19    | CIV18    | CIV17    | CIV16    |
| 12h      | CIV15    | CIV14    | CIV13    | CIV12    | CIV11    | CIV10    | CIV9     | CIV8     |
| 13h      | CIV7     | CIV6     | CIV5     | CIV4     | CIV3     | CIV2     | CIV1     | CIV0     |
| 14h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HDTV     |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | M/S*     | MCP      | PCM      | XCM      |
| 1Dh      | Reserved | BLKEN    | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | GOENB1   | GOENB0   | GPIOL1   | GPIOL0   | Reserved | Reserved | POUTE    | POUTP    |
| 1Fh      | IBS      | DES      | SYO      | VSP      | HSP      | IDF2     | IDF1     | IDF0     |
| 20h      | Reserved | XOSC2    | Reserved | DACT3    | DACT2    | DACT1    | DACT0    | SENSE    |
| 21h      | XOSC1    | XOSC0    | Reserved | SYNCO1   | SYNCO0   | DACG1    | DACG0    | DACBP    |
| 22h      | Reserved | Reserved | Reserved | BCOEN    | BCOP     | BCO2     | BCO1     | BCO0     |
| 48h      | GPSS     | VSGLN    | Reserved | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 49h      | Reserved | Reserved | Reserved | DACPD3   | DACPD2   | DACPD1   | DACPD0   | TVPD     |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 4Fh      | PEDL7    | PEDL6    | PEDL5    | PEDL4    | PEDL3    | PEDL2    | PEDL1    | PEDL0    |

Table 5: Non-Macrovision registers map of the CH7017

| Register | Bit 7   | Bit 6   | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|----------|---------|---------|--------|--------|--------|--------|--------|--------|
| 00h      | IR2     | IR1     | IR0    | VOS1   | VOS0   | SR2    | SR1    | SR0    |
| 01h      | VOF1    | VOF0    | CFF1   | CFF0   | YFFH1  | YFFH0  | YFFL1  | YFFL0  |
| 02h      | VBID    | CFRB    | CVBW   | CBW    | YSV1   | YSV0   | YCV1   | YCV0   |
| 03h      | PTSEL1  | PTSEL0  | SAV8   | HP8    | VP8    | TE2    | TE1    | TE0    |
| 04h      | SAV7    | SAV6    | SAV5   | SAV4   | SAV3   | SAV2   | SAV1   | SAV0   |
| 05h      | HP7     | HP6     | HP5    | HP4    | HP3    | HP2    | HP1    | HP0    |
| 06h      | VP7     | VP6     | VP5    | VP4    | VP3    | VP2    | VP1    | VP0    |
| 07h      | BL7     | BL6     | BL5    | BL4    | BL3    | BL2    | BL1    | BL0    |
| 08h      |         |         |        |        |        | CE2    | CE1    | CE0    |
| 09h      | MEM2    | MEM1    | MEM0   | N9     | N8     | M8     | PLLCPI | PLLCAP |
| 0Ah      | M7      | M6      | M5     | M4     | M3     | M2     | M1     | M0     |
| 0Bh      | N7      | N6      | N5     | N4     | N3     | N2     | N1     | N0     |
| 0Ch      | FSCI31  | FSCI30  | FSCI29 | FSCI28 | FSCI27 | FSCI26 | FSCI25 | FSCI24 |
| 0Dh      | FSCI23  | FSCI22  | FSCI21 | FSCI20 | FSCI19 | FSCI18 | FSCI17 | FSCI16 |
| 0Eh      | FSCI15  | FSCI14  | FSCI13 | FSCI12 | FSCI11 | FSCI10 | FSCI9  | FSCI8  |
| 0Fh      | FSCI7   | FSCI6   | FSCI5  | FSCI4  | FSCI3  | FSCI2  | FSCI1  | FSCI0  |
| 10h      | STFDEN1 | STFDEN0 | CIV25  | CIV24  | CIVC1  | CIVC0  | PALN   | CIVEN  |
| 11h      | CIV23   | CIV22   | CIV21  | CIV20  | CIV19  | CIV18  | CIV17  | CIV16  |
| 12h      | CIV15   | CIV14   | CIV13  | CIV12  | CIV11  | CIV10  | CIV9   | CIV8   |
| 13h      | CIV7    | CIV6    | CIV5   | CIV4   | CIV3   | CIV2   | CIV1   | CIV0   |
| 14h      | BGBST   |         |        |        |        |        |        |        |
| 1Ch      |         | IBS2    | MCP2   | XCM2   | M/S*   | MCP1   | PCM    | XCM1   |
| 1Dh      |         | BLKEN   |        |        | X1CMD3 | X1CMD2 | X1CMD1 | X1CMD0 |
| 1Eh      | GOENB1  | GOENB0  | GPIOL1 | GPIOL0 | HPIR   | HPIE   | POUTE  | POUTP  |
| 1Fh      | IBS1    | DES     | SYOTV  | VSPTV  | HSPTV  | IDF12  | IDF11  | IDF10  |
| 20h      |         | XOSC2   | HPI    | DACT3  | DACT2  | DACT1  | DACT0  | SENSE  |
| 21h      | XOSC1   | XOSC0   | IDF13  | SYNCO1 | SYNCO0 | DACG1  | DACG0  | DACBP  |
| 22h      | SHF2    | SHF1    | SHF0   | BCOEN  | BCOP   | BCO2   | BCO1   | BCO0   |
| 47h      | DVS     |         |        |        |        |        |        |        |

|     |         |         |         |         |         |         |         |         |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| 48h |         |         | TVPLL   | ResetIB | ResetDB |         | TSTP1   | TSTP0   |
| 49h |         |         | TV      | DACPD3  | DACPD2  | DACPD1  | DACPD0  | TVPD    |
| 4Ah | VID7    | VID6    | VID5    | VID4    | VID3    | VID2    | VID1    | VID0    |
| 4Bh | DID7    | DID6    | DID5    | DID4    | DID3    | DID2    | DID1    | DID0    |
| 53h | X2CMD3  | X2CMD2  | X2CMD1  | X2CMD0  | IDF23   | IDF22   | IDF21   | IDF20   |
| 55h | USC7    | USC6    | USC5    | USC4    | USC3    | USC2    | USC1    | USC0    |
| 56h | USC15   | USC14   | USC13   | USC12   | USC11   | USC10   | USC9    | USC8    |
| 57h | USC23   | USC22   | USC21   | USC20   | USC19   | USC18   | USC17   | USC16   |
| 58h | USC31   | USC30   | USC29   | USC28   | USC27   | USC26   | USC25   | USC24   |
| 59h | USC39   | USC38   | USC37   | USC36   | USC35   | USC34   | USC33   | USC32   |
| 5Ah | USVIV7  | USVIV6  | USVIV5  | USVIV4  | USVIV3  | USVIV2  | USVIV1  | USVIV0  |
| 5Bh | USVIV15 | USVIV14 | USVIV13 | USVIV12 | USVIV11 | USVIV10 | USVIV8  | USVIV8  |
| 5Ch | C5GP2   | C5GP1   | C5GP0   |         | USHIV17 | USHIV16 | USHIV17 | USHIV16 |
| 5Dh | USHIV7  | USHIV6  | USHIV5  | USHIV4  | USHIV3  | USHIV2  | USHIV1  | USHIV0  |
| 5Eh | USHIV15 | USHIV14 | USHIV13 | USHIV12 | USHIV11 | USHIV10 | USHIV9  | USHIV8  |
| 5Fh | HAPI7   | HAPI6   | HAPI5   | HAPI4   | HAPI3   | HAPI2   | HAPI1   | HAPI0   |
| 60h | STFDS1  | STFDS0  | VALO10  | VALO9   | VALO8   | HAPI10  | HAPI9   | HAPI8   |
| 61h | VALO7   | VALO6   | VALO5   | VALO4   | VALO3   | VALO2   | VALO1   | VALO0   |
| 62h | HAPO7   | HAPO6   | HAPO5   | HAPO4   | HAPO3   | HAPO2   | HAPO1   | HAPO0   |
| 63h | US      | LVDSPD  |         |         |         | HAPO10  | HAP09   | HAP08   |
| 64h | HVEN    |         | LVDS24  | LVSDC   | LDD     | LDM2D   | LEOSWP  | LDI     |
| 65h | C5GP5   | C5GP4   | C5GP3   | LA3RL   | LA6RL   | LA7RL   | LCNTLE  | LCNTLF  |
| 66h |         | SYNCST  | BKLEN   | LPLEN   | LPFORC  | LPLOCK  | LSYNCEN | PANEN   |
| 67h | TPON7   | TPON6   | TPON5   | TPON4   | TPON3   | TPON2   | TPON1   | TPON0   |
| 68h | TPON8   | TPBLE6  | TPBLE5  | TPBLE4  | TPBLE3  | TPBLE2  | TPBLE1  | TPBLE0  |
| 69h | TPOFF8  | TPBLD6  | TPBLD5  | TPBLD4  | TPBLD3  | TPBLD2  | TPBLD1  | TPBLD0  |
| 6Ah | TPOFF7  | TPOFF6  | TPOFF5  | TPOFF4  | TPOFF3  | TPOFF2  | TPOFF1  | TPOFF0  |
| 6Bh | C4GP5   | C4GP4   | TPPWD5  | TPPWD4  | TPPWD3  | TPPWD2  | TPPWD1  | TPPWD0  |
| 6Ch | C4GP3   | C4GP2   | GPIODR5 | GPIODR4 | GPIODR3 | GPIODR2 | GPIODR1 | GPIODR0 |
| 6Dh | C4GP1   | C4GP0   | C3GP5   | C3GP4   | GPIOL5  | GPIOL4  | GPIOL3  | GPIOL2  |
| 6Eh | C3GP3   | C3GP2   | C3GP1   | C3GP0   | GOENB5  | GOENB4  | GOENB3  | GOENB2  |
| 71h |         |         | LPFFD1  | LPFFD0  | LPFBD3  | LPFBD2  | LPFBD1  | LPFBD0  |
| 72h |         |         | LPPSD1  | LPPSD0  | LPVCO3  | LPVCO2  | LPVCO1  | LPVCO0  |
| 73h | LSP2    | DAS1    | DAS0    | LDEN1   | LDEN0   | LPCP2   | LPCP1   | LPCP0   |
| 74h | LODP    | LODPE   | L2ODA2  | L2ODA1  | L2ODA0  | L1ODA2  | L1ODA1  | L1ODA0  |
| 75h | LODST   |         |         |         |         |         |         |         |
| 76h | FRSTB   |         |         |         | LPPDN   | LPPRB   | LODPDB1 | LODPDB0 |
| 78h |         | LPLF4   | LPLF3   | LPPD4   | LPPD3   | LPPD2   | LPPD1   | LPPD0   |
| 7Fh | BGLMT7  | BGLMT6  | BGLMT5  | BGLMT4  | BGLMT3  | BGLMT2  | BGLMT1  | BGLMT0  |

Table 6: Non-Macrovision registers map of the CH7019

| Register | Bit 7   | Bit 6   | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|----------|---------|---------|--------|--------|--------|--------|--------|--------|
| 00h      | IR2     | IR1     | IR0    | VOS1   | VOS0   | SR2    | SR1    | SR0    |
| 01h      | VOF1    | VOF0    | CFF1   | CFF0   | YFFH1  | YFFH0  | YFFL1  | YFFL0  |
| 02h      | VBID    | CFRB    | CVBW   | CBW    | YSV1   | YSV0   | YCV1   | YCV0   |
| 03h      | PTSEL1  | PTSEL0  | SAV8   | HP8    | VP8    | TE2    | TE1    | TE0    |
| 04h      | SAV7    | SAV6    | SAV5   | SAV4   | SAV3   | SAV2   | SAV1   | SAV0   |
| 05h      | HP7     | HP6     | HP5    | HP4    | HP3    | HP2    | HP1    | HP0    |
| 06h      | VP7     | VP6     | VP5    | VP4    | VP3    | VP2    | VP1    | VP0    |
| 07h      | BL7     | BL6     | BL5    | BL4    | BL3    | BL2    | BL1    | BL0    |
| 08h      |         |         |        |        |        | CE2    | CE1    | CE0    |
| 09h      | MEM2    | MEM1    | MEM0   | N9     | N8     | M8     | PLLCP1 | PLLCP0 |
| 0Ah      | M7      | M6      | M5     | M4     | M3     | M2     | M1     | M0     |
| 0Bh      | N7      | N6      | N5     | N4     | N3     | N2     | N1     | N0     |
| 0Ch      | FSCI31  | FSCI30  | FSCI29 | FSCI28 | FSCI27 | FSCI26 | FSCI25 | FSCI24 |
| 0Dh      | FSCI23  | FSCI22  | FSCI21 | FSCI20 | FSCI19 | FSCI18 | FSCI17 | FSCI16 |
| 0Eh      | FSCI15  | FSCI14  | FSCI13 | FSCI12 | FSCI11 | FSCI10 | FSCI9  | FSCI8  |
| 0Fh      | FSCI7   | FSCI6   | FSCI5  | FSCI4  | FSCI3  | FSCI2  | FSCI1  | FSCI0  |
| 10h      | STFDEN1 | STFDEN0 | CIV25  | CIV24  | CIVC1  | CIVC0  | PALN   | CIVEN  |
| 11h      | CIV23   | CIV22   | CIV21  | CIV20  | CIV19  | CIV18  | CIV17  | CIV16  |
| 12h      | CIV15   | CIV14   | CIV13  | CIV12  | CIV11  | CIV10  | CIV9   | CIV8   |
| 13h      | CIV7    | CIV6    | CIV5   | CIV4   | CIV3   | CIV2   | CIV1   | CIV0   |
| 14h      | BGBST   |         |        |        |        |        |        |        |
| 1Ch      |         | IBS2    | MCP2   | XCM2   | M/S*   | MCP1   | PCM    | XCM1   |
| 1Dh      |         | BLKEN   |        |        | X1CMD3 | X1CMD2 | X1CMD1 | X1CMD0 |
| 1Eh      | GOENB1  | GOENB0  | GPIOL1 | GPIOL0 |        |        | POUTE  | POUTP  |
| 1Fh      | IBS1    | DES     | SYOTV  | VSPTV  | HSPTV  | IDF12  | IDF11  | IDF10  |

|     |        |        |         |         |         |         |         |         |
|-----|--------|--------|---------|---------|---------|---------|---------|---------|
| 20h |        | XOSC2  |         | DACT3   | DACT2   | DACT1   | DACT0   | SENSE   |
| 21h | XOSC1  | XOSC0  | IDF13   | SYNCO1  | SYNCO0  | DACG1   | DACG0   | DACBP   |
| 22h |        |        |         | BCOEN   | BCOP    | BCO2    | BCO1    | BCO0    |
| 23h |        |        |         |         |         |         |         | PEDLEN  |
| 47h | DVS    |        |         |         |         |         |         |         |
| 48h |        |        | TVPLL   | ResetIB | ResetDB |         | TSTP1   | TSTP0   |
| 49h |        |        | TV      | DACPD3  | DACPD2  | DACPD1  | DACPD0  | TVPD    |
| 4Ah | VID7   | VID6   | VID5    | VID4    | VID3    | VID2    | VID1    | VID0    |
| 4Bh | DID7   | DID6   | DID5    | DID4    | DID3    | DID2    | DID1    | DID0    |
| 4Fh | PEDL7  | PEDL6  | PEDL5   | PEDL4   | PEDL3   | PEDL2   | PEDL1   | PEDL0   |
| 53h | X2CMD3 | X2CMD2 | X2CMD1  | X2CMD0  | IDF23   | IDF22   | IDF21   | IDF20   |
| 5Ch | C5GP2  | C5GP1  | C5GP0   | PSR     |         |         |         |         |
| 60h | STFDS1 | STFDS0 |         |         |         |         |         |         |
| 63h |        | LVDSPD |         |         |         |         |         |         |
| 64h |        |        | LVDS24  | LVSDC   | LDD     | LDM2D   | LEOSWP  |         |
| 65h | C5GP5  | C5GP4  | C5GP3   |         | LA6RL   |         | LCNTLE  | LCNTLF  |
| 66h |        | SYNCST | BKLEN   | LPLEN   | LPFORC  | LPLOCK  | LSYNCEN | PANEN   |
| 67h | TPON7  | TPON6  | TPON5   | TPON4   | TPON3   | TPON2   | TPON1   | TPON0   |
| 68h | TPON8  | TPBLE6 | TPBLE5  | TPBLE4  | TPBLE3  | TPBLE2  | TPBLE1  | TPBLE0  |
| 69h | TPOFF8 | TPBLD6 | TPBLD5  | TPBLD4  | TPBLD3  | TPBLD2  | TPBLD1  | TPBLD0  |
| 6Ah | TPOFF7 | TPOFF6 | TPOFF5  | TPOFF4  | TPOFF3  | TPOFF2  | TPOFF1  | TPOFF0  |
| 6Bh | C4GP5  | C4GP4  | TPPWD5  | TPPWD4  | TPPWD3  | TPPWD2  | TPPWD1  | TPPWD0  |
| 6Ch | C4GP3  | C4GP2  | GPIODR5 | GPIODR4 | GPIODR3 | GPIODR2 | GPIODR1 | GPIODR0 |
| 6Dh | C4GP1  | C4GP0  | C3GP5   | C3GP4   | GPIOL5  | GPIOL4  | GPIOL3  | GPIOL2  |
| 6Eh | C3GP3  | C3GP2  | C3GP1   | C3GP0   | GOENB5  | GOENB4  | GOENB3  | GOENB2  |
| 71h |        |        | LPFFD1  | LPFFD0  | LPFBD3  | LPFBD2  | LPFBD1  | LPFBD0  |
| 72h |        |        | LPPSD1  | LPPSD0  | LPVCO3  | LPVCO2  | LPVCO1  | LPVCO0  |
| 73h |        |        |         | LDEN1   | LDEN0   | LPCP2   | LPCP1   | LPCP0   |
| 74h | LODP   | LODPE  | L2ODA2  | L2ODA1  | L2ODA0  | L1ODA2  | L1ODA1  | L1ODA0  |
| 75h | LODST  |        |         |         |         |         |         |         |
| 76h | FRSTB  |        |         |         | LPPDN   | LPPRB   | LODPDB1 | LODPDB0 |
| 78h |        | LPLF4  | LPLF3   | LPPD4   | LPPD3   | LPPD2   | LPPD1   | LPPD0   |
| 7Fh | BGLMT7 | BGLMT6 | BGLMT5  | BGLMT4  | BGLMT3  | BGLMT2  | BGLMT1  | BGLMT0  |

Table 7: Serial Port Register Map of the CH7304

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 14h      | Reserved | Reserved | Reserved | Reserved | Reserved | CLKDETD  | Reserved | Reserved |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | Reserved | MCP      | Reserved | XCM      |
| 1Dh      | Reserved | Reserved | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | Reserved | GOENB    | Reserved | GPIOL    | Reserved | Reserved | Reserved | Reserved |
| 1Fh      | IBS      | Reserved | Reserved | Reserved | Reserved | IDF2     | IDF1     | IDF0     |
| 31h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | RGB      |
| 48h      | Reserved | Reserved | Reserved | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 63h      | Reserved | LVDSPD   | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 64h      | Reserved | Reserved | LVDS24   | Reserved | LDD      | Reserved | LEOSWP   | LDI      |
| 66h      | Reserved | SYNCST   | BKLEN    | LPLEN    | LPFORC   | LPLOCK   | LSYNCEN  | PANEN    |
| 67h      | TPON7    | TPON6    | TPON5    | TPON4    | TPON3    | TPON2    | TPON1    | TPON0    |
| 68h      | TPON8    | TPBLE6   | TPBLE5   | TPBLE4   | TPBLE3   | TPBLE2   | TPBLE1   | TPBLE0   |
| 69h      | TPOFF8   | TPBLD6   | TPBLD5   | TPBLD4   | TPBLD3   | TPBLD2   | TPBLD1   | TPBLD0   |
| 6Ah      | TPOFF7   | TPOFF6   | TPOFF5   | TPOFF4   | TPOFF3   | TPOFF2   | TPOFF1   | TPOFF0   |
| 6Bh      | Reserved | Reserved | TPPWD5   | TPPWD4   | TPPWD3   | TPPWD2   | TPPWD1   | TPPWD0   |
| 71h      | Reserved | Reserved | LPFFD1   | LPFFD0   | LPFBD3   | LPFBD2   | LPFBD1   | LPFBD0   |
| 72h      | Reserved | Reserved | LPPSD1   | LPPSD0   | LPVCO3   | LPVCO2   | LPVCO1   | LPVCO0   |
| 73h      | Reserved | Reserved | Reserved | LDEN1    | LDEN0    | LPCP2    | LPCP1    | LPCP0    |
| 74h      | LODP     | LODPE    | Reserved | Reserved | Reserved | LODA2    | LODA1    | LODA0    |
| 75h      | LODST    | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 76h      | FRSTB    | LPLF2    | LPLF1    | LPLF0    | LPPDN    | LPPRB    | LODPDB1  | LODPDB0  |
| 78h      | LPCP3    | LPLF4    | LPLF3    | LPPD4    | LPPD3    | LPPD2    | LPPD1    | LPPD0    |
| 7Fh      | BGLMT7   | BGLMT6   | BGLMT5   | BGLMT4   | BGLMT3   | BGLMT2   | BGLMT1   | BGLMT0   |

**Table 8: Serial Port Register Map for the CH7305**

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 14h      | Reserved | Reserved | Reserved | Reserved | Reserved | CLKDETD  | Reserved | Reserved |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | Reserved | MCP      | Reserved | XCM      |
| 1Dh      | Reserved | Reserved | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | Reserved | GOENB    | Reserved | GPIOL    | Reserved | Reserved | Reserved | Reserved |
| 1Fh      | IBS      | Reserved | Reserved | Reserved | Reserved | IDF2     | IDF1     | IDF0     |
| 31h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | RGB      |
| 48h      | Reserved | Reserved | Reserved | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 63h      | Reserved | LVDSPD   | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 64h      | Reserved | Reserved | LVDS24   | LVSDSC   | LDD      | Reserved | LEOSWP   | LDI      |
| 65h      | Reserved | Reserved | Reserved | LA3RL    | LA6RL    | LA7RL    | LCNTLE   | LCNTLF   |
| 66h      | Reserved | SYNCST   | BKLEN    | LPLEN    | LPFORC   | LPLOCK   | LSYNCEN  | PANEN    |
| 67h      | TPON7    | TPON6    | TPON5    | TPON4    | TPON3    | TPON2    | TPON1    | TPON0    |
| 68h      | TPON8    | TPBLE6   | TPBLE5   | TPBLE4   | TPBLE3   | TPBLE2   | TPBLE1   | TPBLE0   |
| 69h      | TPOFF8   | TPBLD6   | TPBLD5   | TPBLD4   | TPBLD3   | TPBLD2   | TPBLD1   | TPBLD0   |
| 6Ah      | TPOFF7   | TPOFF6   | TPOFF5   | TPOFF4   | TPOFF3   | TPOFF2   | TPOFF1   | TPOFF0   |
| 6Bh      | Reserved | Reserved | TPPWD5   | TPPWD4   | TPPWD3   | TPPWD2   | TPPWD1   | TPPWD0   |
| 71h      | Reserved | Reserved | LPFFD1   | LPFFD0   | LPFBD3   | LPFBD2   | LPFBD1   | LPFBD0   |
| 72h      | Reserved | Reserved | LPPSD1   | LPPSD0   | LPVCO3   | LPVCO2   | LPVCO1   | LPVCO0   |
| 73h      | Reserved | Reserved | Reserved | LDEN1    | LDEN0    | LPCP2    | LPCP1    | LPCP0    |
| 74h      | LODP     | LODPE    | L2ODA2   | L2ODA1   | L2ODA0   | L1ODA2   | L1ODA1   | L1ODA0   |
| 75h      | LODST    | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 76h      | FRSTB    | LPLF2    | LPLF1    | LPLF0    | LPPDN    | LPPRB    | LODPDB1  | LODPDB0  |
| 78h      | LPCP3    | LPLF4    | LPLF3    | LPPD4    | LPPD3    | LPPD2    | LPPD1    | LPPD0    |
| 7Fh      | BGLMT7   | BGLMT6   | BGLMT5   | BGLMT4   | BGLMT3   | BGLMT2   | BGLMT1   | BGLMT0   |

**Table 9: Serial Port Register Map for the CH7301C**

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 1Ch      |          |          |          |          |          | MCP      |          | XCM      |
| 1Dh      |          |          |          |          | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | GOENB1   | GOENB0   | GPIOL1   | GPIOL0   | HPIR     | HPIE     |          |          |
| 1Fh      |          |          |          |          |          | IDF2     | IDF1     | IDF0     |
| 20h      | HPIE2    | XOSC2    | DVIT     |          | DACT2    | DACT1    | DACT0    | SENSE    |
| 21h      | XOSC1    | XOSC0    |          |          | SYNCO0   | DACG1    | DACG0    | DACBP    |
| 23h      |          |          |          |          |          | HPDD     |          |          |
| 31h      | TPPD3    | TPPD2    | TPPD1    | TPPD0    | CTL3     | CTL2     | CTL1     | CTL0     |
| 33h      | DVID2    | DVID1    | DVID0    | DVII     | Reserved | Reserved | Reserved | TPCP0    |
| 34h      |          | TPLLB    | TPFFD1   | TPFFD0   | TPFBD3   | TPFBD2   | TPFBD1   | TPFBD0   |
| 35h      | Reserved | Reserved | TPVT5    | TPVT4    | TPVT3    | TPVT2    | TPVT1    | TPVT0    |
| 36h      | TPLPF3   | TPLPF2   | TPLPF1   | TPLPF0   | Reserved | Reserved | Reserved | Reserved |
| 37h      | TPVCO10  | TPVCO9   | TPVCO8   | Reserved | Reserved | Reserved | Reserved | Reserved |
| 48h      |          |          |          | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 49h      | DVIP     | DVIL     | Reserved | Reserved | DACPD2   | DACPD1   | DACPD0   | FPD      |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |

**Table 10: Serial Port Register Map for the CH7303**

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00h      | IR2      | IR1      | IR0      | VOS1     | VOS0     | SR2      | SR1      | SR0      |
| 03h      | Reserved | Reserved | Reserved | HP8      | VP8      | Reserved | Reserved | Reserved |
| 05h      | HP7      | HP6      | HP5      | HP4      | HP3      | HP2      | HP1      | HP0      |
| 06h      | VP7      | VP6      | VP5      | VP4      | VP3      | VP2      | VP1      | VP0      |
| 07h      | BL7      | BL6      | BL5      | BL4      | BL3      | BL2      | BL1      | BL0      |
| 14h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HDTV     |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | Reserved | MCP      | Reserved | XCM      |
| 1Dh      | Reserved | Reserved | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Eh      | GOENB1   | GOENB0   | GPIOL1   | GPIOL0   | HPIR     | Reserved | Reserved | Reserved |
| 1Fh      | Reserved | DES      | Reserved | VSP      | HSP      | IDF2     | IDF1     | IDF0     |
| 20h      | HPIE     | Reserved | DVIT     | Reserved | DACT2    | DACT1    | DACT0    | SENSE    |
| 21h      | Reserved | Reserved | IDF3     | Reserved | SYNCO    | DACG1    | DACG0    | DACBP    |
| 23h      | Reserved | Reserved | Reserved | Reserved | Reserved | HPDD     | Reserved | Reserved |
| 31h      | Reserved | Reserved | Reserved | Reserved | CTL3     | CTL2     | CTL1     | CTL0     |
| 33h      | DVID2    | DVID1    | DVID0    | DVII     | TPPSD1   | TPPSD0   | Reserved | TPCP0    |
| 34h      | Reserved | Reserved | TPFFD1   | TPFFD0   | TPFBD3   | TPFBD2   | TPFBD1   | TPFBD0   |
| 36h      | TPLPF3   | TPLPF2   | TPLPF1   | TPLPF0   | Reserved | Reserved | Reserved | Reserved |
| 48h      | Reserved | Reserved | Reserved | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 49h      | DVIP     | DVIL     | Reserved | Reserved | DACPD2   | DACPD1   | DACPD0   | FPD      |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 56h      | Reserved | Reserved | TMSYO    | Reserved | Reserved | Reserved | Reserved | T_RGB    |

**Table 11: Serial Port Register Map for the CH7310**

| Register | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00h      | IR2      | IR1      | IR0      | VOS1     | VOS0     | SR2      | SR1      | SR0      |
| 03h      | Reserved | Reserved | Reserved | HP8      | VP8      | Reserved | Reserved | Reserved |
| 05h      | HP7      | HP6      | HP5      | HP4      | HP3      | HP2      | HP1      | HP0      |
| 06h      | VP7      | VP6      | VP5      | VP4      | VP3      | VP2      | VP1      | VP0      |
| 07h      | BL7      | BL6      | BL5      | BL4      | BL3      | BL2      | BL1      | BL0      |
| 14h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HDTV     |
| 1Ch      | Reserved | Reserved | Reserved | Reserved | Reserved | MCP      | Reserved | XCM      |
| 1Dh      | Reserved | Reserved | Reserved | Reserved | XCMD3    | XCMD2    | XCMD1    | XCMD0    |
| 1Fh      | Reserved | DES      | Reserved | VSP      | HSP      | IDF2     | IDF1     | IDF0     |
| 20h      | Reserved | Reserved | Reserved | Reserved | DACT2    | DACT1    | DACT0    | SENSE    |
| 21h      | Reserved | Reserved | IDF3     | Reserved | SYNCO    | DACG1    | DACG0    | DACBP    |
| 48h      | Reserved | Reserved | Reserved | ResetIB  | ResetDB  | Reserved | TSTP1    | TSTP0    |
| 49h      | Reserved | Reserved | Reserved | Reserved | DACPD2   | DACPD1   | DACPD0   | FPD      |
| 4Ah      | VID7     | VID6     | VID5     | VID4     | VID3     | VID2     | VID1     | VID0     |
| 4Bh      | DID7     | DID6     | DID5     | DID4     | DID3     | DID2     | DID1     | DID0     |
| 56h      | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | T_RGB    |

**4. Revision History**

| <b>Rev. #</b> | <b>Date</b> | <b>Section</b> | <b>Description</b>                                      |
|---------------|-------------|----------------|---|
| 1.0           | 10/18/02    | All            | First official release.                                 |
| 1.1           | 2/07/03     | All            | Added CH7304/CH7305 to the scope of the document        |
| 1.2           | 3/5/03      | 3.0            | Added Electrical Specifications of the serial interface |
| 1.3           | 4/24/03     | All            | Added CH7301C/CH7303 to the scope of the document       |
| 1.4           | 7/12/04     | All            | Added CH7310 device to the document                     |

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