

PCB Layout and Design Considerations for the CH7301C DVI Output Device

1. Introduction

This application note focuses on basic PCB layout and design guidelines for the CH7301C DVI Output Device. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for DVI link implementation, are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of CH7301C. Please refer to CH7301C data sheet for the details of the pin assignments.

2. Component Placement and Design Considerations

Components associated with the CH7301C DVI transmitter should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1 μ F ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C7, C8, C9, C11, C12, C14, C17) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7301C ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7301C should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7301C ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage DVDDV), DVI, Analog, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment in CH7301C

Pin #	# of Pins	Type	Symbol	Description
1, 12, 49	3	Power	DVDD	Digital Supply Voltage (3.3V)
6, 11, 64	3	Power	DGND	Digital Ground
45	1	Power	DVDDV	I/O Supply Voltage (1.1V to 3.3V)
23, 29	2	Power	TVDD	DVI Transmitter Supply Voltage (3.3V)
20, 26, 32	3	Power	TGND	DVI Transmitter Ground
18	1	Power	AVDD	PLL Supply Voltage (3.3V)
16, 17	2	Power	AGND	PLL Ground
33	1	Power	VDD	DAC Supply Voltage (3.3V)
34, 40	2	Power	GND	DAC Ground

• DVDDV & VREF Decoupling and Connection

VREF is used as a reference level for pixel data input D[11:0], HSYNC input and VSYNC input. Please refer to **Figure 1** for optimum decoupling. In general applications, VREF is derived from DVDDV divided by 2, i.e., $VREF = 1/2 \times DVDDV$.

Therefore, in **Figure 2**, both resistors should have the same value ($10K\Omega @ 1\%$). The decoupling capacitor is required as shown in **Figure 2**. Also, the DVDDV voltage supply should be connected to the graphics controller I/O supply voltage.

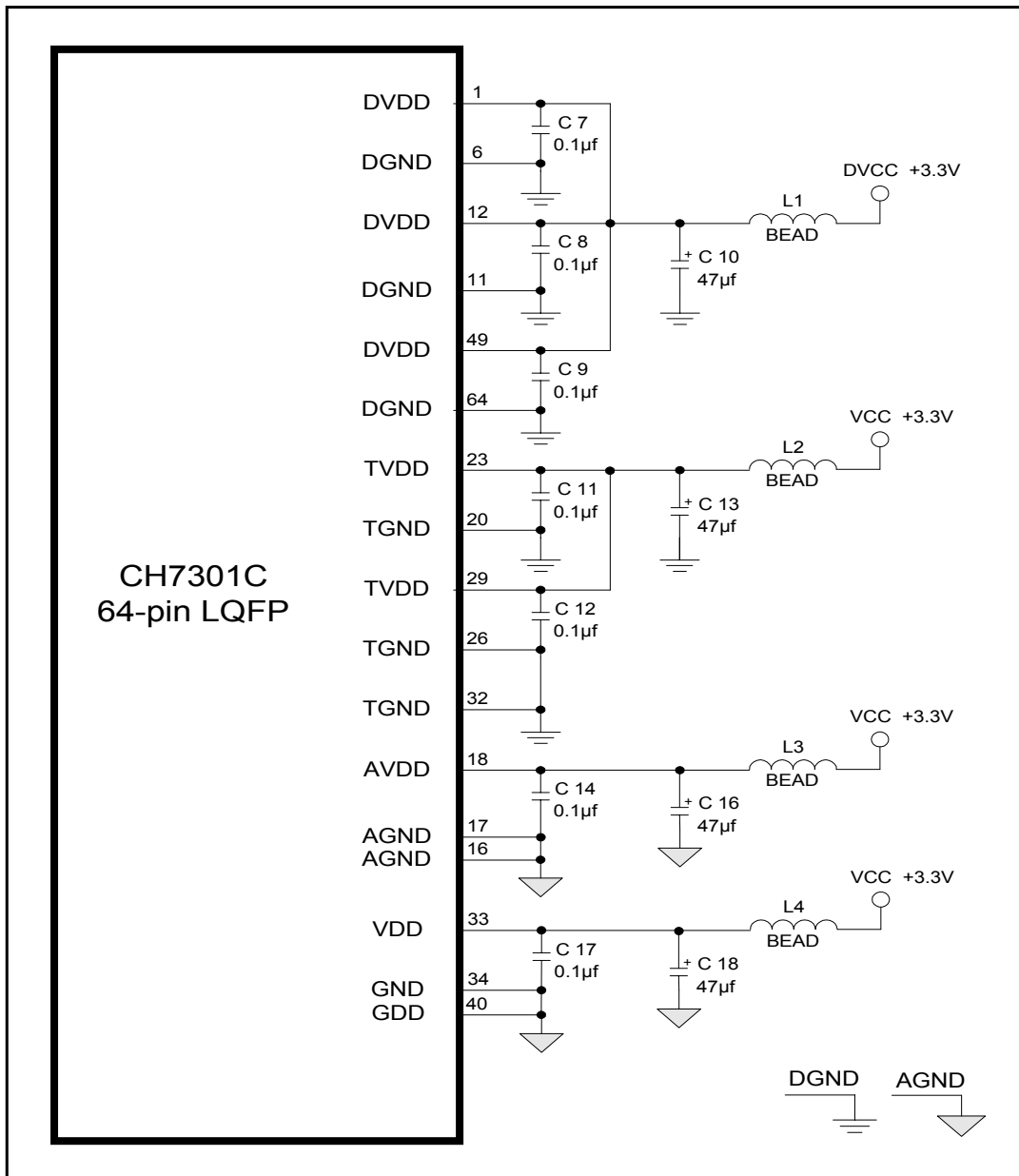


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

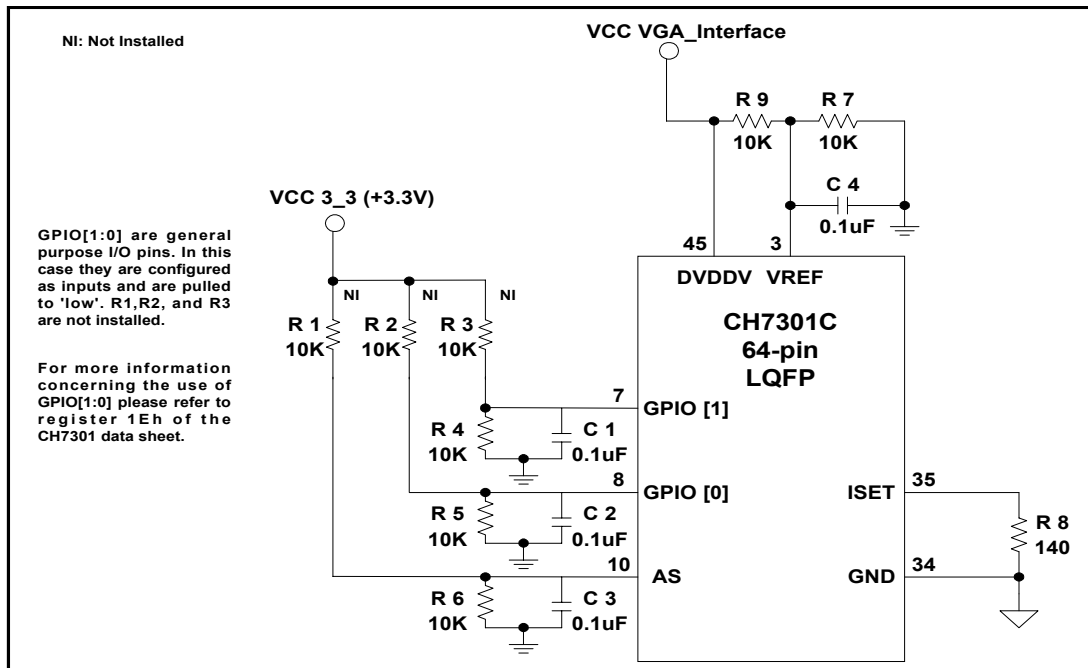


Figure 2: ISET, VREF, DVDDV, GPIO and AS connection

2.2 General Control

- **ISET pin**

The ISET pin, pin 35, sets the DAC current. A 140Ω resistor should be placed as close as possible to the ISET pin using short and wide traces. Whenever possible, the ISET resistor ground pin should also be connected to pin 34. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7301C. See **Figure 2** for design reference.

- **Data Enable pin**

The Data Enable pin, pin 2, is an input pin and accepts the Data Enable signal from the VGA graphics chipset. Active video data is indicated when the VGA drives the Data Enable signal 'high'. When the Data Enable signal is 'low', the video data will not be encoded and driven out of the DVI interface. The voltage levels are between 0V and DVDDV, and the VREF signal is used as the threshold level.

- **GPIO [0] & GPIO[1] pins**

GPIO[1:0] are General Purpose I/O pins. To set the direction of these pins, register 1Eh, the GPIO Control Register must be set accordingly. The GPIO[1] pin can be configured as an output for the DVI link detect signal. In this configuration, this pin will be driven low when a termination change has been detected on the HPDET input.

- **AS pin**

The Address Select pin, pin 10, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled 'low', then the serial port address is 0x76h, if AS is pulled 'high', then the serial port address is 0x75h.

Note: To use the Intel driver for the CH7301C, the AS pin must be pulled 'low'.

- **Video Inputs (D[11:0])**

Since the digital pixel data and the pixel clock of the CH7301C may toggle at speeds up to 165MHz (depending on the input mode), it is critical that the connection of these video signals between the graphics controller and the CH7301C be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

2.3 Serial Port Interface

- **SPD and SPC pins**

SPD (pin 14) and SPC (pin 15) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 2.2 KΩ resistors.

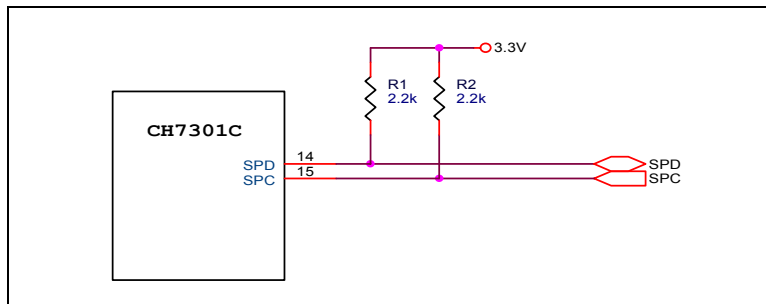


Figure 3: Serial Port Interface

2.4 DVI Output and Control

In DVI output mode, the multiplexed input data, sync and clock signals are input to the CH7301C from the graphics controller’s digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

The TDC0, TDC1, TDC2 & TLC signals are high frequency differential signals that need to be routed with special precautions. Since the TDC0, TDC1, TDC2 & TLC signals are differential they must be routed in pairs: TDC0 & TDC0*, TDC1 & TDC1*, TDC2 & TDC2*, TLC & TLC* signals. The lengths of the 4 pair of signals must be kept as close to the same as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the DVI connector without any vias to the bottom layer. The pin placement of the TDC0, TDC1, TDC2 & TLC signals allows for a direct route to the DVI connector. The CH7301C is able to drive a DVI display at a pixel rate of up to 165 MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

Figure 4 shows an example of the connection of the DVI output. In the figure a DVI-I Right Angle Connector is used to interface the CH7301C DVI outputs to the monitor.

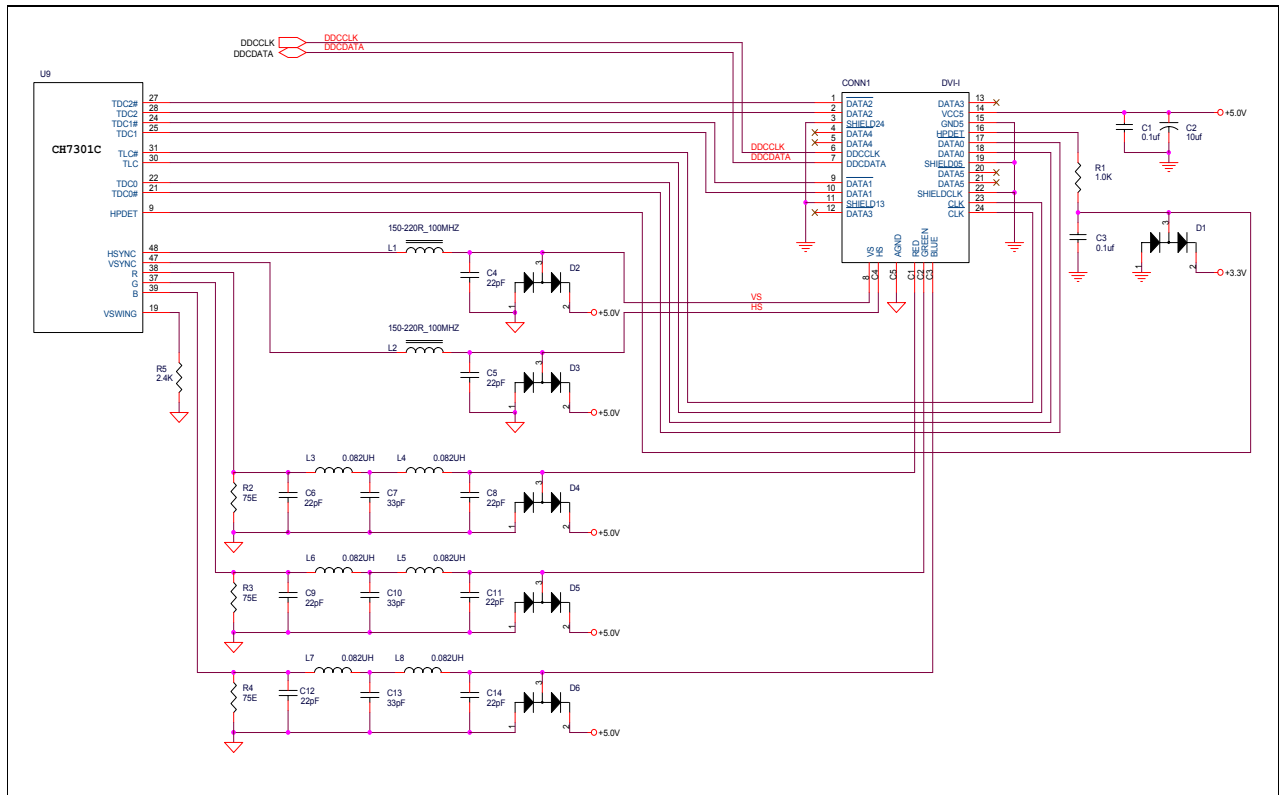


Figure 4: DVI-I Output Connection

- **DVI Link Detect Output (HPINT) (internal pull-up)**

The GPIO[1]/HPINT pin can be used to output the DVI link detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. To configure the GPIO[1]/HPINT pin to function as a HPINT, the GOENB1 (reg 1Eh[7]) and HPIE2 (reg 20h[7]) bits of the CH7301C must be set to 1. The HPINT function will pull low with an open drain output following a transition on the HPDET input.

- **DVI Data Channel (TDC[2:0] and TDC[2:0]*)**

These pins (Pins 28, 25, 22 for TDC[2:0] and Pins 27, 24, 21 for TDC[2:0]*) provide the DVI differential outputs for data channel 0 (blue), channel 1 (green) and channel 2 (red) (See **Figure 4**).

- **DVI Link Clock Outputs (TLC and TLC*)**

These pins (Pins 30, 31) provide the DVI differential clock outputs for the DVI interface corresponding to data on the TDC[2:0] outputs (See **Figure 4**).

- **HPDET (DVI Hot Plug Detect)**

This input pin (Pin 9) determines whether the DVI link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the GPIO[1]/HPINT pin pulling low (See **Figure 4**).

- **VSWING (DVI Link Swing Control)**

This pin (Pin 19) sets the swing level of the DVI outputs. A 2.4K Ω resistor should be connected between this pin and GND using short and wide traces.

2.5 Analog RGB Output

The R, G, B (pins 38, 37, 39) signals are analog video signals. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the R, G, B signals and 20 mils spacing between them and any digital trace.

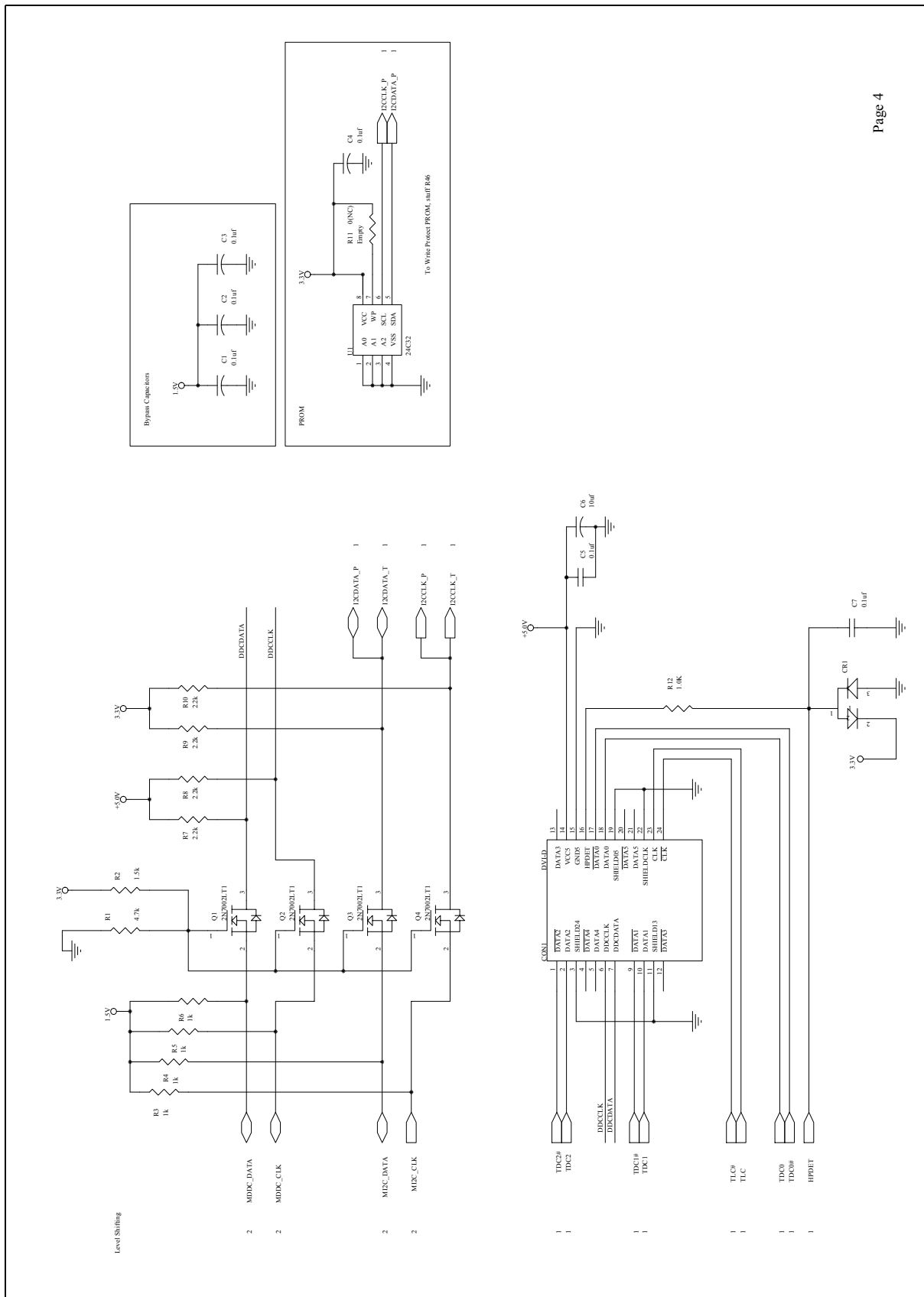
Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corners should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them.

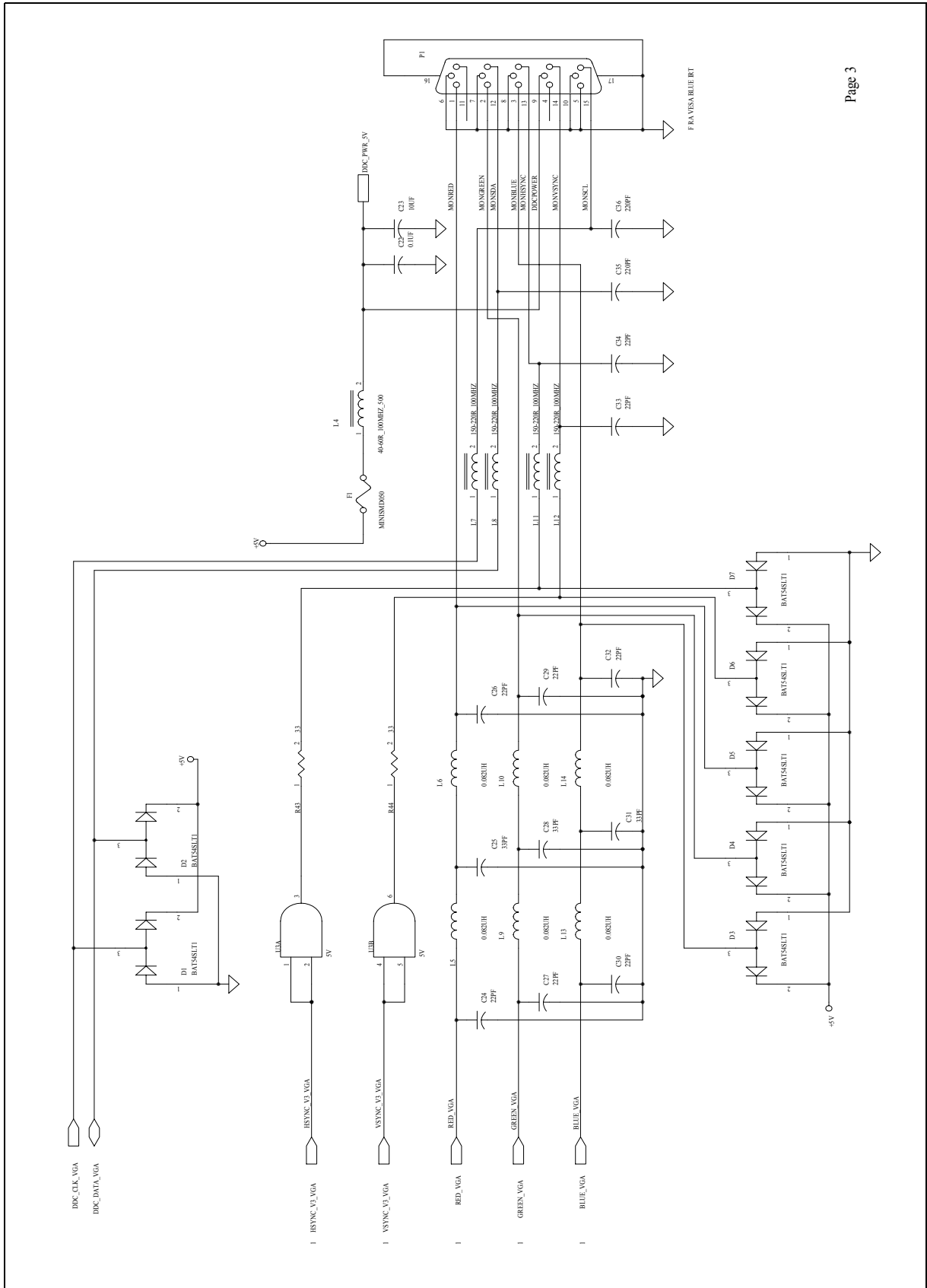
In **Figure 4**, the input protection diodes D1 - D6 should be placed as close to the DVI connector as possible and the series termination resistors R2-R4 should be placed as close to the CH7301C as possible. If the analog outputs of the DVI-I connector are to be used, the ferrite beads L1-L8 should be placed as close to the DVI-I connector as possible to reduce EMI emissions.

3. Reference Design Example

The following schematics are based on an Intel Brookdale[®] / Montara[®] / Springdale[®] Graphics chipset design and are to be used as a CH7301C PCB design example only. It is not a complete design. Those who are seriously doing an application design with CH7301C and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example





4. Revision History

Revision	Date	Section	Description
1.0	7/23/03	All	First official release, Revision 1.0

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Chrontel

**2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com**

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