

PCB Layout and Design Considerations for CH7019B LVDS/TV Output Device

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7019B LVDS/TV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for both LVDS and TV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures shown in this document are based on the 128-pin LQFP package of CH7019B designed with an Intel® i865 graphics chipset.

2. Component Placement

Components associated with the CH7019B encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7019B ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7019B should be separate but eventually connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7019B ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage VDDV), PLL, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment

Pin #	# of pins	Type	Symbol	Description
64, 83, 84, 103	4	Power	DVDD	Digital Supply Voltage (3.3V)
67, 75, 92, 100	4	Power	DGND	Digital Ground
60	1	Power	VDDV	I/O Supply Voltage (1.1V to 3.3V)
55	1	Power	TVPLL_VDD	TV PLL Supply Voltage (3.3V)
54	1	Power	TVPLL_VCC	TV PLL Supply Voltage (3.3V)
51	1	Power	TVPLL_GND	TV PLL Ground
37	1	Power	DAC_VDD	DAC Supply Voltage (3.3V)
39, 48	2	Power	DAC_GND	DAC Ground
7, 13, 19, 20, 26, 32	6	Power	LVDD	LVDS Supply Voltage (3.3V)
4, 10, 16, 23, 29, 35	6	Power	LGND	LVDS Ground
1	1	Power	LPLL_VDD	LVDS PLL Supply Voltage (3.3V)
3	1	Power	LPLL_GND	LVDS PLL Ground

• **Digital, DAC and PLL Power Pins Decoupling and Connection**

Figure 1 shows the decoupling and connection for the LPLL_VDD, LVDD, DAC_VDD, TVPLL_VCC, TVPLL_VDD and DVDD.

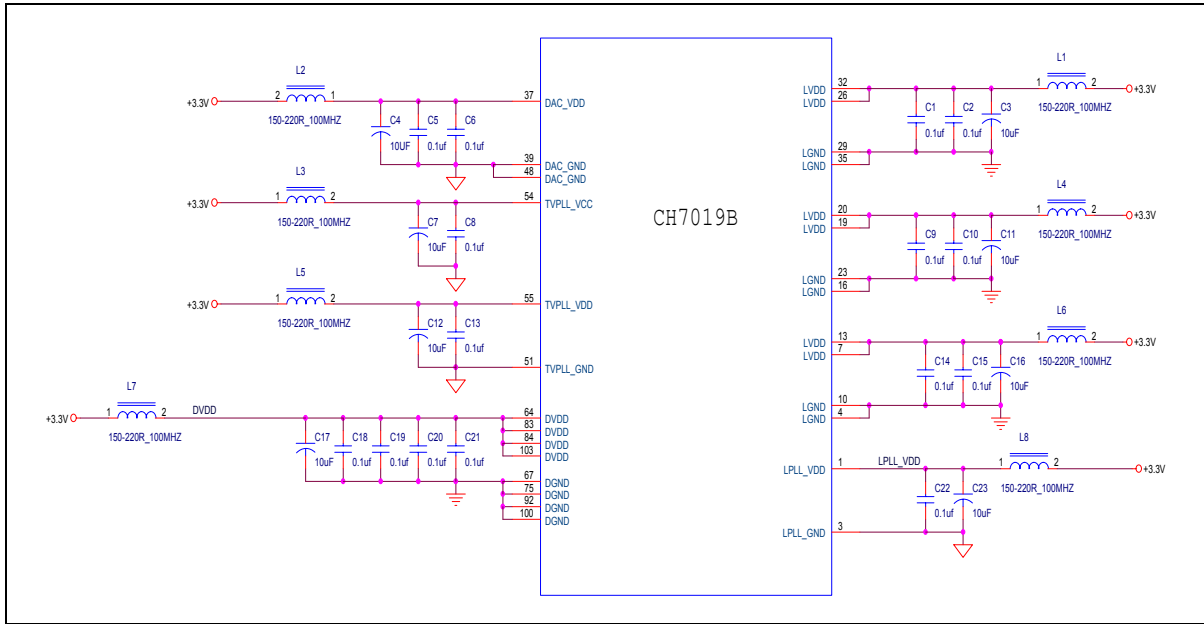


Figure 1: Digital, DAC and PLL Power pins Decoupling and Connection

Note: All the Ferrite Beads described in this document are recommended to have $<.05 \Omega$ at DC; $2 \text{ } 3\Omega$ at 25MHz & 47Ω at 100MHz. Please refer to Fair-Rite part# 2743019447 for detail or an equivalent part can be used for the diagram.

• **VDDV and VREF1, VREF2 Decoupling and Connection**

VDDV is I/O supply voltage (1.1V to 3.3V), which makes the amplitude of I/O signals from 0V to VDDV.

VREF1 inputs a reference voltage of $VDDV/2$. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, syncs and clock inputs. Please refer to **Figure 2** for the decoupling and connection.

VREF2 should be tied externally to the maximum voltage seen by the SPD and SPC ports (1.5V to 3.3V).

Figure 2 shows the decoupling and connection for the VDDV, VREF1, and VREF2.

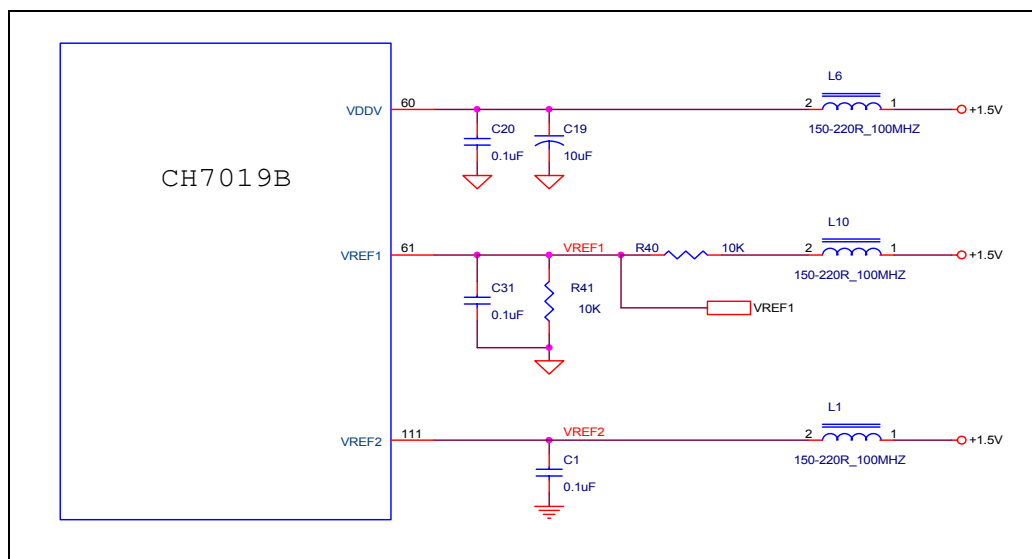


Figure 2: VDDV, VREF1, and VREF2 pins Decoupling and Connection

2.2 General Control

- **ISET Pin**

A 140 Ω resistor should be placed directly and as close as possible to Pin 38, ISET, with short and wide traces. Whenever possible, the ISET resistors ground pin should also be connected to the pin 39, DAC ground. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7019B. See **Figure 3** for design reference.

- **GPIO[5:0] Pins**

These pins provide general purpose I/O and are controlled via the serial port. The direction of these signals are controlled by register 6Eh, GPIO Direction Control Register. When the direction is “input”, the GPIO[5:0] pins have a weak pull-up (about 1 MΩ), and can be used to determine the type of panel, the standard/type of TV, etc., during system boot-up. See **Figure 3** for design reference. In the reference design, each GPIO pin is connected with a pair of resistors, which allows the designer to either pull-up or pull-down the pin. Using GPIO[0] (pin 123) as an example, if it should be set to HIGH, R65 can be stuffed with a 10 KΩ resistor, and R66 should not be stuffed. If it is to be set to LOW, then R65 should not be stuffed, and R66 can be stuffed with a 100KΩ resistor.

- **AS pin**

The AS pin has an internal pull-up and determines the device address of the CH7019B for the serial port. The device address is defined as {1 1 1 0 1 AS* AS R/W}. With AS pulled low, the address is {1 1 1 0 1 1 0 R/W}, which is ECh (Write) or EDh (Read). With AS pulled high, the address is {1 1 1 0 1 0 1 R/W}, which is EAh (Write) or EBh (Read).

- **RESET* pin**

The RESET* pin has an internal pull-up. When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

- **LPLLAP pin**

LPLLAP pin allows coupling of any signal to the on-chip loop filter capacitor. A capacitor with a typical value 0.1 nf, should be connected between this pin (pin 2) and the ground (See **Figure 3**).

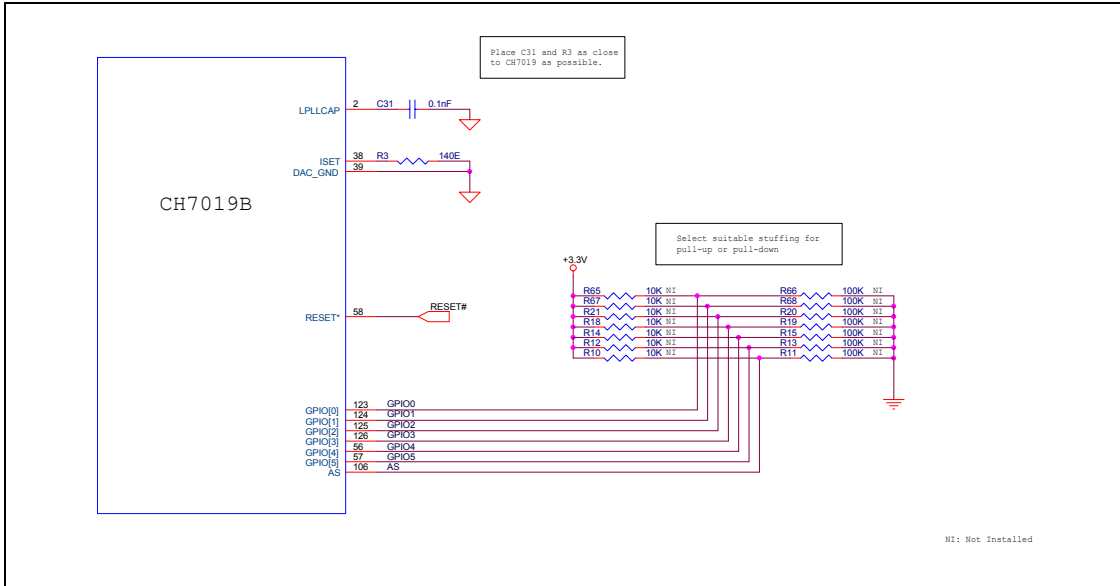


Figure 3: General Control Reference Design

2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

Crystal Input

The 14.31818 MHz (± 20 ppm) crystal must be placed as close as possible to the XI/FIN and XO pins (Pins 52 and 53), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7019B encoder, it is very important that noise does not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7019B pin 51 ground pin.

Reference Crystal Oscillator

The CH7019B includes an oscillator circuit which allows a 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7019B. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and possess low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal required is specified to be 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors must have their ground connection very close to the CH7019B (C_{ext}).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$$

where:

C_{ext} = external load capacitance required on XI/FIN and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7019B (approximately 10-15 pF on each of XI/FIN and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 4** for the symbols used in the calculation described above.

In general, let us assume

$$C_{int \text{ XI/FIN}} = C_{int \text{ XO}} = C_{int}$$

$$C_{ext \text{ XI/FIN}} = C_{ext \text{ XO}} = C_{ext}$$

such that

$$C_L = (C_{int} + C_{ext}) / 2 + C_S \text{ and } C_{ext} = 2(C_L - C_S) - C_{int}$$

$$= 2C_L - (2C_S + C_{int})$$

Therefore C_L must be specified greater than $C_{int} / 2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is **not** operating in an excessive drive level specified by crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For a detail consideration of crystal oscillator design, please refer AN-06.

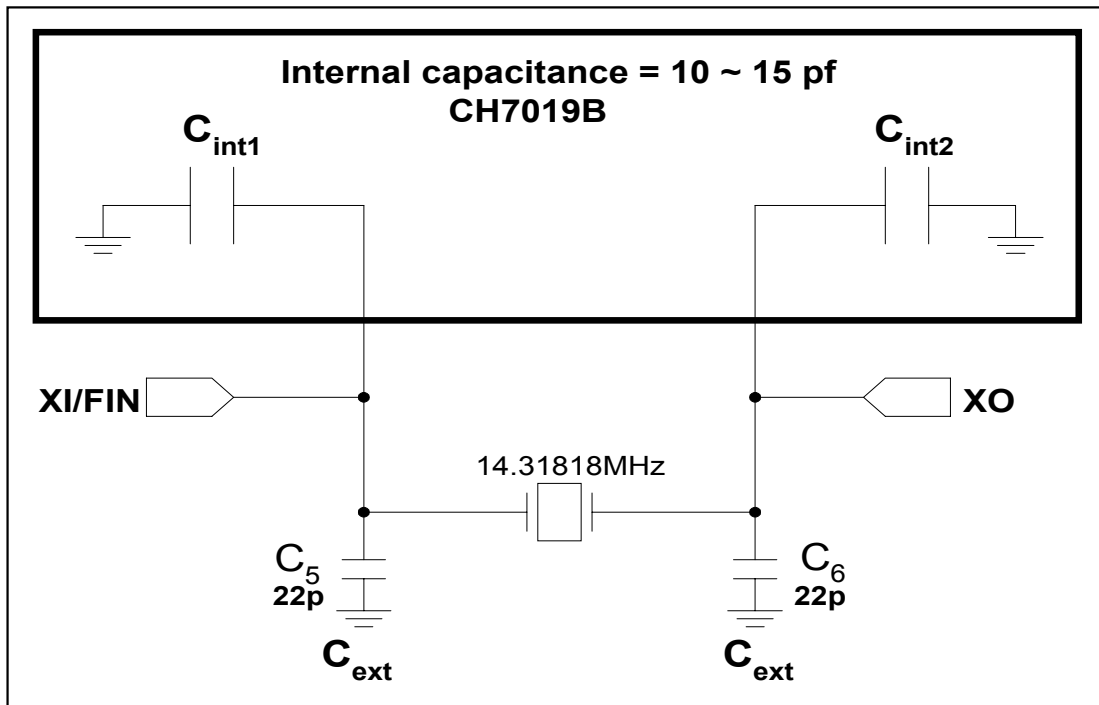


Figure 4: Reference Crystal Design.

- **P-Out pin**

The P-Out pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output driver is driven from the VDDV supply (pin 60). In the reference design, this pin is connected to DVOBC_CLKIN. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.

- **XCLK1, XCLK1*, XCLK2, XCLK2* (External Clocks Input) pins**

XCLK1 and XCLK1* form a differential clock signal input to CH7019B for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF1. In the reference design they are connected to DVOB_CLK and DVOB_CLK# (see **Figure 5** for reference design).

XCLK2 and XCLK2* form a differential clock signal input to CH7019B for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF1. In the reference design they are connected to DVOC_CLK and DVOC_CLK# (see **Figure 5** for reference design).

- **BCO (Buffered Clock Output) pin**

BCO pin (pin 50) provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply. When it is used as a buffered clock out, the BCO register (register 22h) controls the types of the output clocks (see CH7019B datasheet for details). It is very useful for troubleshooting. See TB-37 for the methods of measuring crystal clock and color burst frequencies using BCO pin.

For the reference design of the clock pins, please see **Figure 5**.

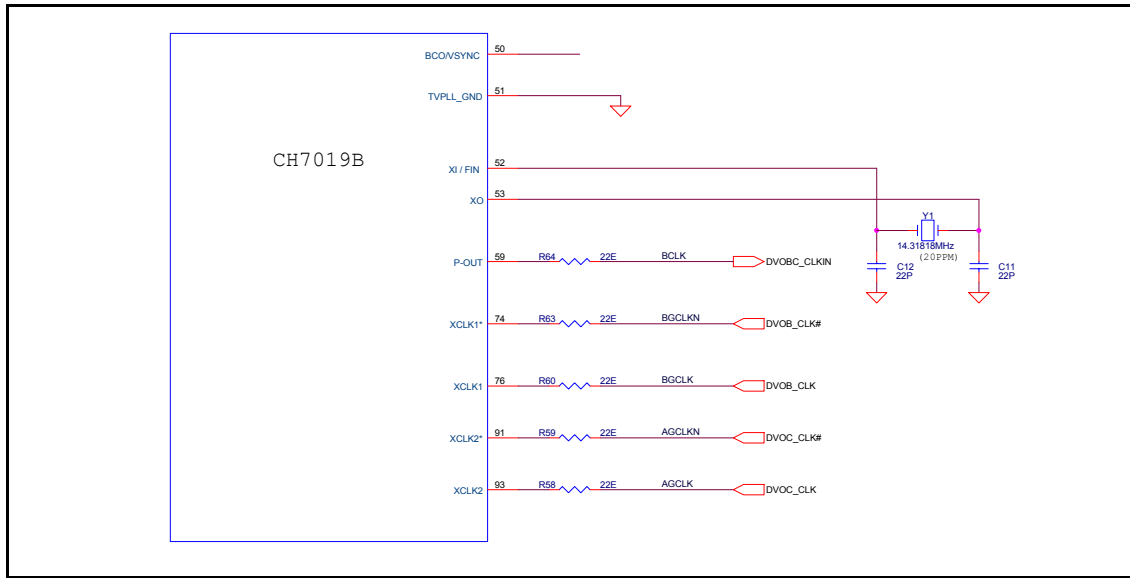


Figure 5: Clock and Crystal Oscillator Reference Design

2.4 Serial Ports Control

- **SPD and SPC pins**

SPD (pin 107) and SPC (pin 108) functions as a bi-directional serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 1 K Ω resistors and are connected directly to SPD and SPC, respectively.

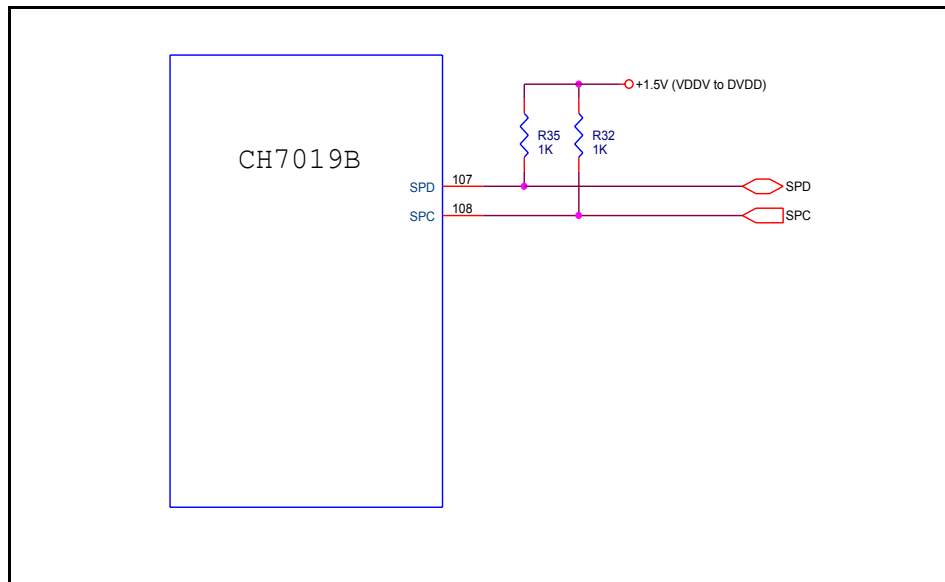


Figure 6: Serial Port Control Reference Design

2.5 Data Input and Syncs

Since the digital pixel data and the pixel clock of the CH7019B may toggle at speeds of up to 165MHz (depending on the input mode), it is critical that the connection of these video input signals between the graphics controller and the CH7019B be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

- **D1[11:0] and D2[11:0]**

Each set of data pins accepts a set of 12 data inputs from a digital video port of a graphics controller. The levels are 0V to VDDV. VREF1 is the threshold level. The two sets of data pins can be ganged together as a single 18 bit data port. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that the trace width of these signals be 8 mils.

- **H1 and V1**

When the SYOTV control bit, Register 1Fh - bit 5, is low, H1 and V1 accept horizontal/vertical sync inputs for use with the D1[11:0] input data. The amplitude will be 0V to VDDV. VREF1 is the threshold level for these inputs.

- **H2 and V2**

When the SYOTV control bit, Register 1Fh - bit 5, is low, H2 and V2 accept horizontal/vertical sync inputs for use with the D2[11:0] input data. The amplitude will be 0V to VDDV. VREF1 is the threshold level for these inputs.

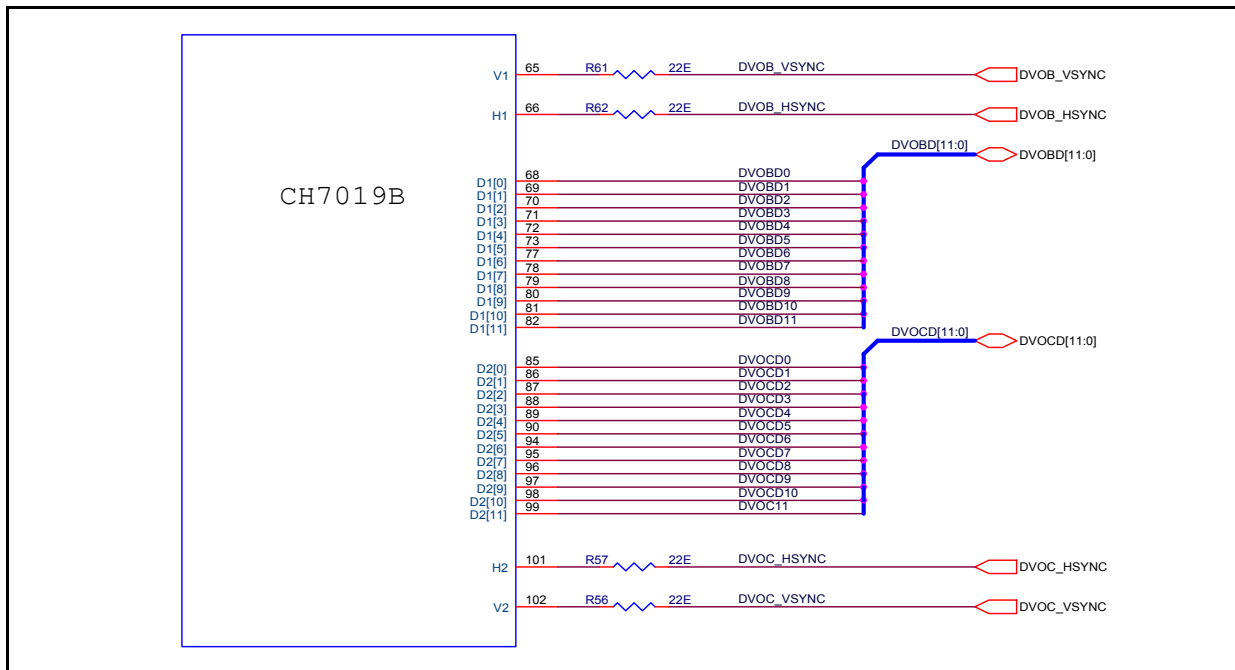


Figure 7: Data Input and Syncs Reference Design

2.6 TV Output and Control

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7019B from the graphics controller’s digital output port. A P-OUT clock can be outputted as the frequency reference to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7019B from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X

times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. **Figure 8** shows the design example for TV out and control.

The components associated with the video output pins should be placed as close as possible to the CH7019B. The 75 Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7019B to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs or Y, Pr and Pb signals should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit elements for a typical S-Video and composite outputs are shown in **Figure 9**, and its corresponding frequency response is shown in **Figures 10 and 11**.

Table 2: TV Output Configurations

	2 RCA + 1 S-Video	SCART
DACA0 (pin 47)	CVBS	B
DACA1 (pin 43)	Y	G
DACA2 (pin 45)	C	R
DACA3 (pin 41)	CVBS	CVBS
	VGA - Bypass RGB	480i YPrPb
DACB0 (pin 46)	B	Pb
DACB1 (pin 42)	G	Y
DACB2 (pin 44)	R	Pr
DACB3 (pin 40)		CVBS

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on the set of DAC output pins, different reconstruction filters for each type of signals can be implemented on the break-out cables. **Figure 12** shows the connection for the SCART output.

When RGB bypass mode is selected, pin 49, C/HSYNC, and pin 50, BCO/VSYNC, provide horizontal sync and vertical sync, respectively, for the RGB display monitor.

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each DAC connecting to TV (Refer to AN-38 for details).

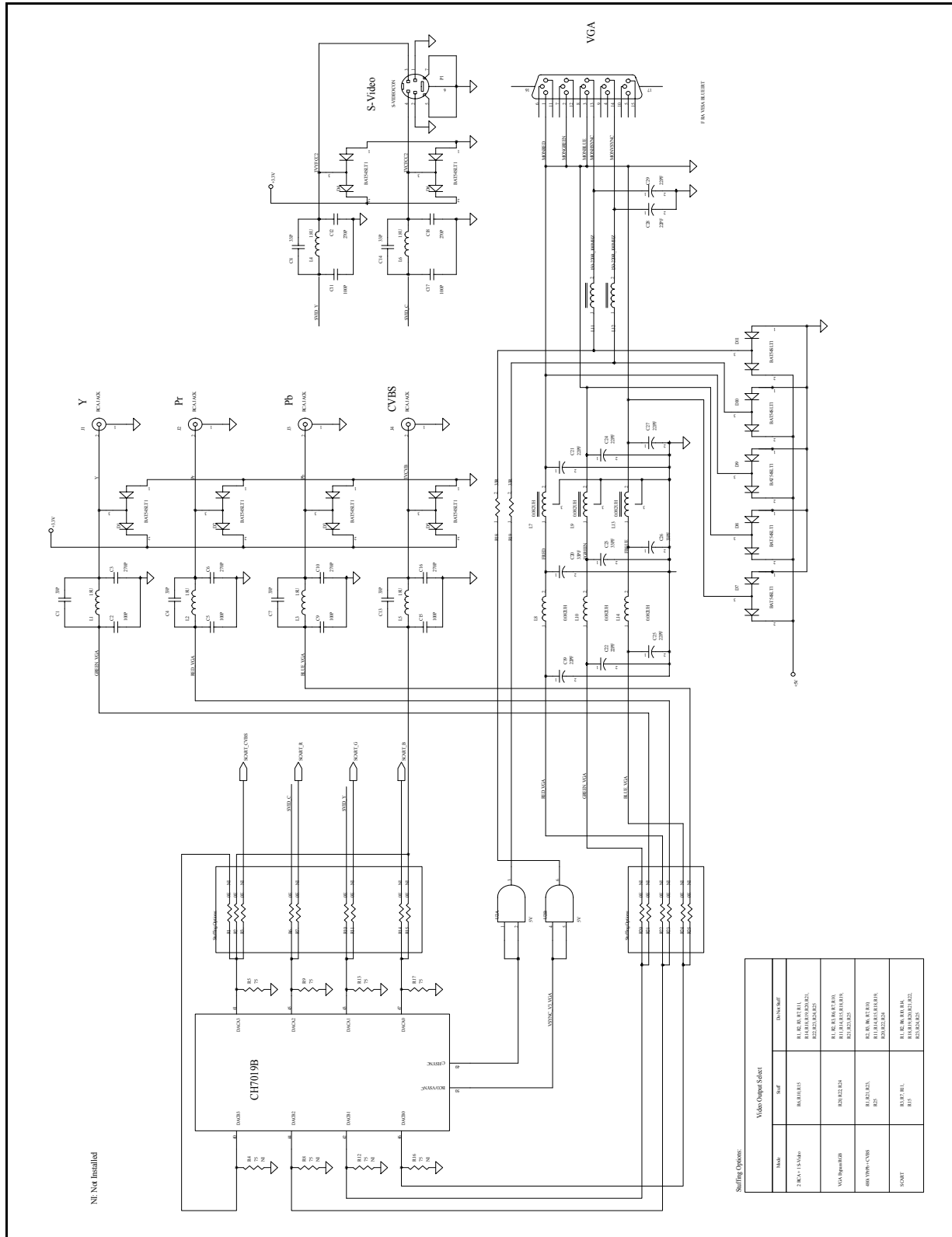


Figure 8: TV Output and Control Reference Design

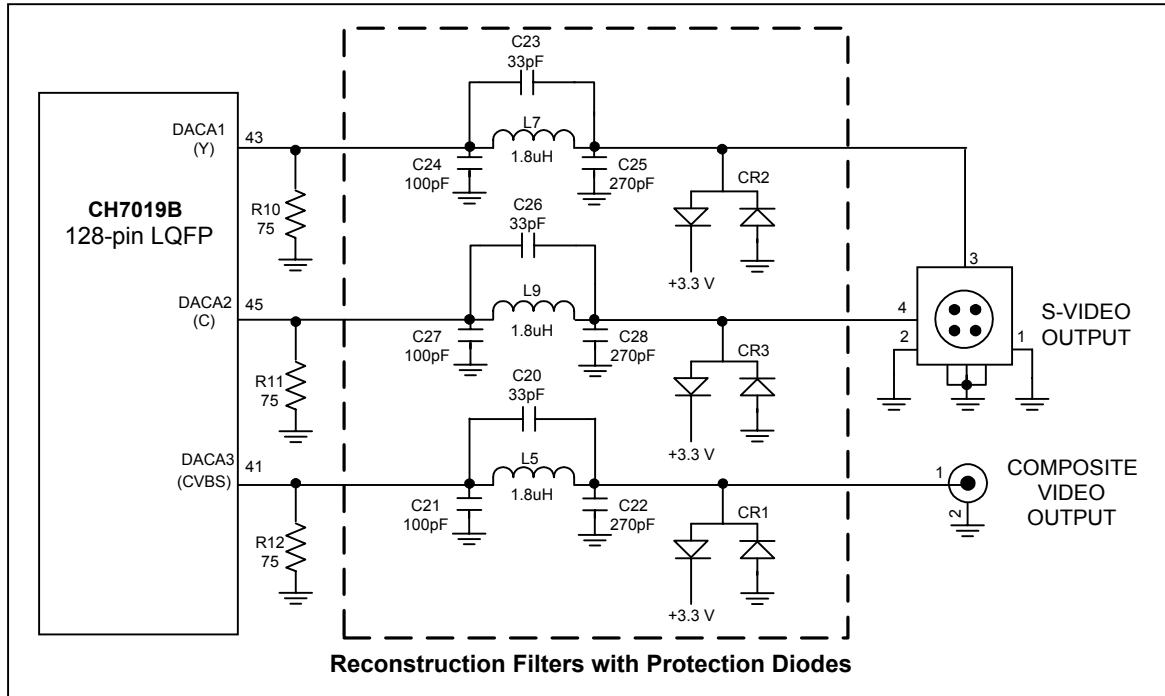


Figure 9: The Typical Connection For the S-Video and Composite Outputs

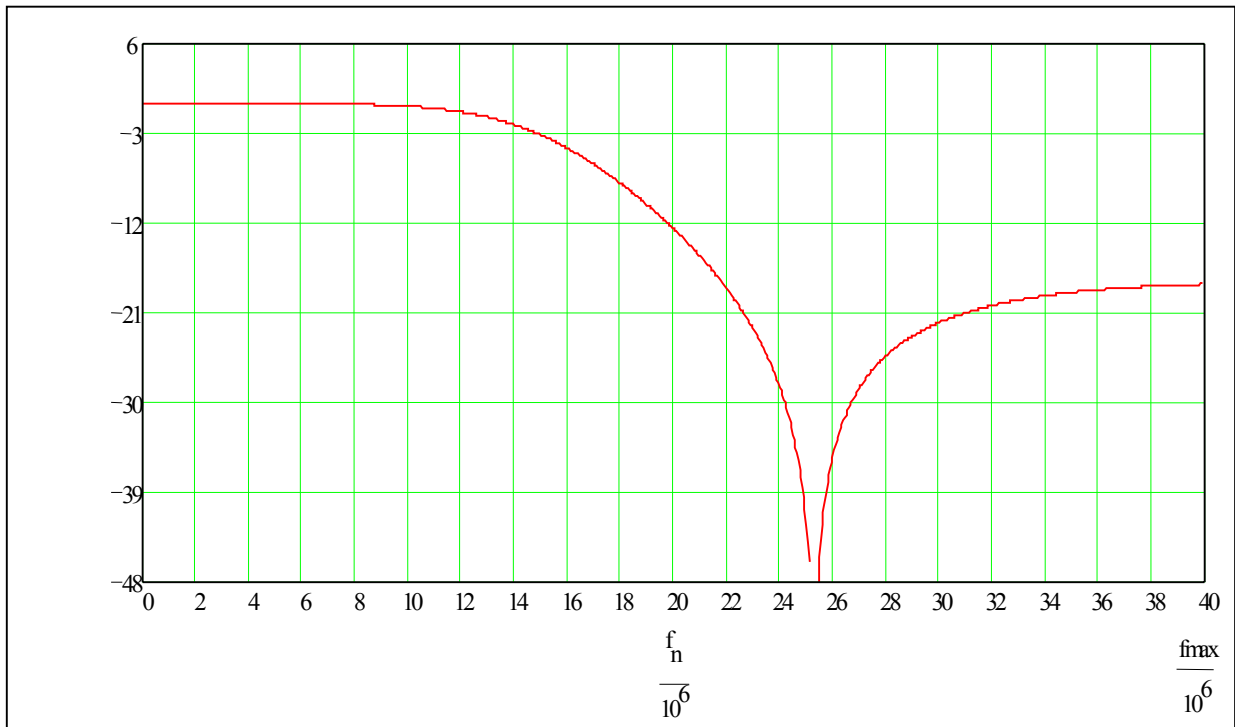


Figure 10: Amplitude Response of the 3rd Order Reconstruction Filter

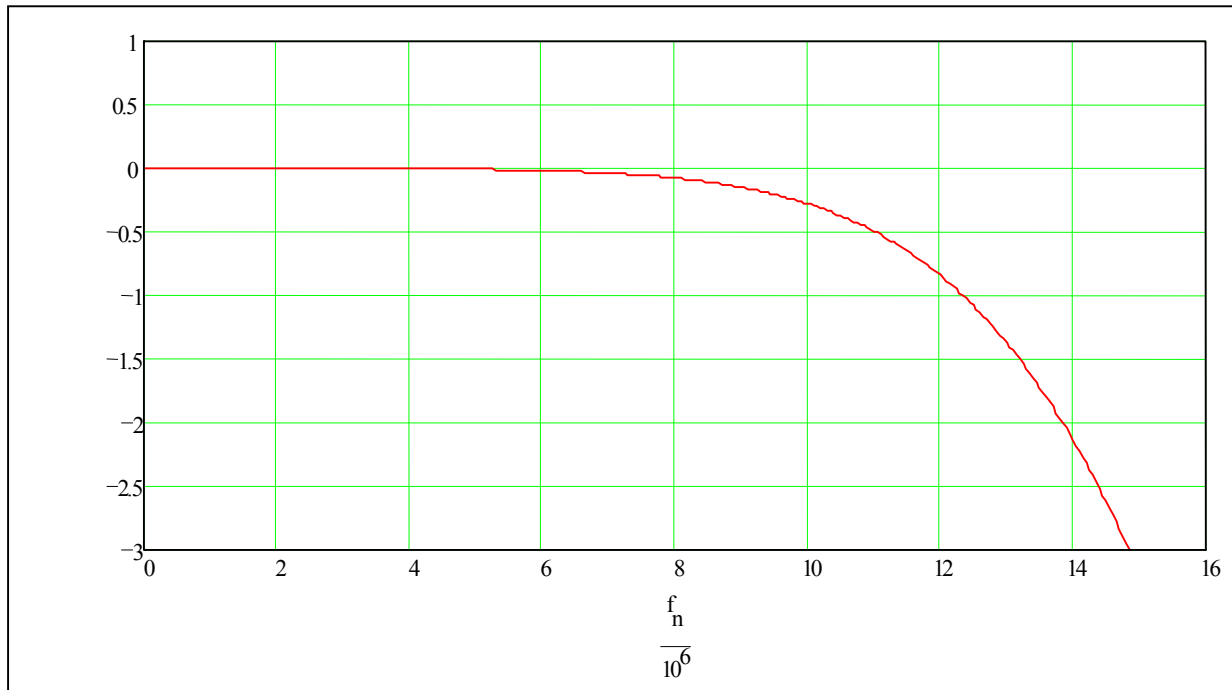


Figure 11: The Details of the Amplitude Response of the Pass Band

Note: If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN-46 on how to achieve the desired configuration.

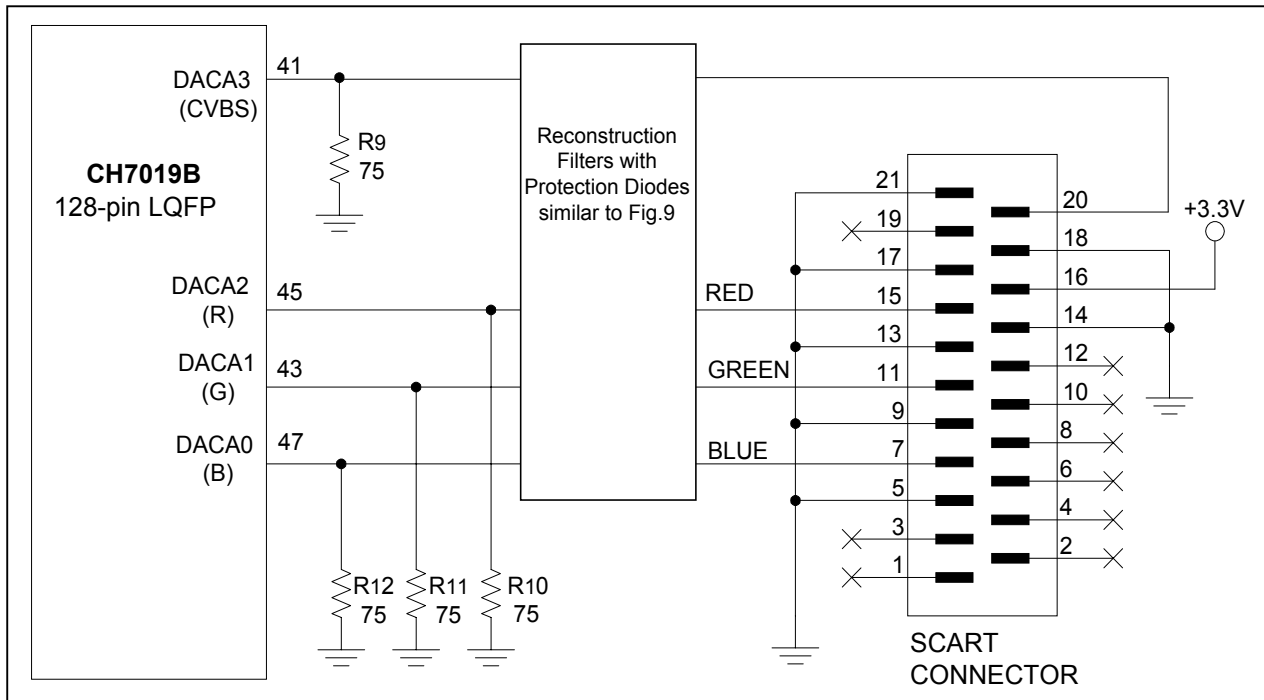


Figure 12: The Connection for the SCART Connector

Careful layout consideration for the CVBS, Y and C (or CVBS, R, G and B) traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

2.7 LVDS Output and Control

The LVDS Output pins include: LDC[6:4], LDC[2:0], LL1C, LL1C*, LL2C, LL2C*. The LVDS Control pins include: VSWING, FLD1, FLD2, DE1, DE2, ENAVDD and ENABKL. The connection of the pins are described as follows. **Figure 13** shows a reference design example for LVDS output and control.

- **VSWING**

VSWING is the LVDS swing control. This pin sets the swing level of the LVDS outputs. A 2.4 K Ω resistor should be connected between this pin and LGND (pin 35) using short and wide traces.

- **FLD1, FLD2**

FLD1 and FLD2 are tri-stated upon power-up.

- **DE1, DE2**

DE1 and DE2 are Data Enable control pins for Channel 1 and Channel 2, respectively.

These pins accept a Data Enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0V to VDDV. VREF1 is the threshold level. In the reference design, these pins are connected to VADE and VBDE, respectively.

- **ENAVDD, ENABKL**

ENAVDD (pin127) and ENABKL (pin 128) are for LVDS panel power control: ENAVDD enables the panel's 3.3 v VDD and ENABKL enables the panel's back-light. In the reference design, the pins are connected to the panel's VDD and backlight control circuits respectively.

- **LDC[6:4], LDC[2:0], LL1C, LL1C*, LL2C, LL2C***

The LDC[6:4], LDC[2:0], LL1C, LL1C*, LL2C, LL2C* signals are high frequency differential signals that need to be routed with special precautions. They must be routed in pairs with the length as close as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less while using 45 degree corner angles. These signals should be routed on the top layer directly to the connector without any vias to the bottom layer. The traces for the LVDS signals should be closely coupled and should have a 100 Ω differential impedance (50 Ω to the ground from each differential pin).

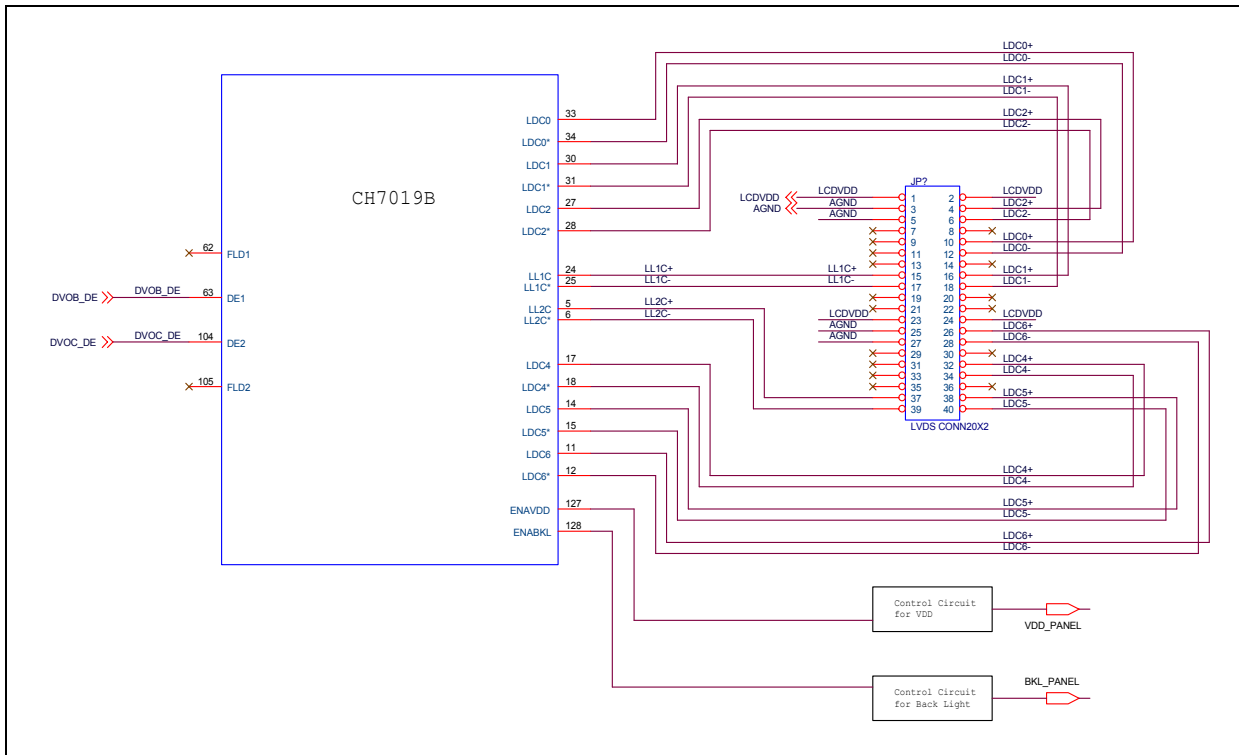


Figure 13: LVDS Output and Control Reference Design

3. LVDS Output Design Tips

Output and Control Reference Design

- Dedicating planes for Vcc and Ground are typically required for high-speed design. The solid ground plane is required to establish a controlled impedance for the transmission line interconnects. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance.
- If it is possible, put CMOS/TTL signals and LVDS signals on different layers which should be isolated by the power and ground planes.
- Power and ground should use wide (low impedance) traces. Do not use 50Ω design rules on power and ground traces.
- Keep ground PCB return paths short and wide. Provide a return path that creates the smallest loop for the image currents to return.
- Traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance. This not only reduces EMI, but also helps to ensure that the noise coupled onto the conductors will be common-mode noise.
- Leave all unused LVDS and CMOS/TTL output open. Do not tie them to ground.
- Tie unused transmitter inputs and control/enable signals to power or ground.

4. Reference Design Example

The following schematics are of a CH7019B PCB design used as an example only. It is not a complete design. Those who are seriously doing an application design using the CH7019B and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

4.1 Schematics of Reference Design Example

CHRONTEL CH7019B REFERENCE SCHEMATIC
FOR
Intel Springdale

Confidential Document

Design File: CH7017_ADD_SPRINGDALE_IP01.DSN

Sheet NO	Content
1	Title Page
2	Assembly Instruction
3	AGP Connector
4	CH7019 Interface
5	Panel Powers
6	Open DI Connector
7	VGa Bypass RGB Mode
8	YPrPb

Revision History:

This Schematic is CHRONTEL Confidential and issued under NDA only.

DISCLAIMER
The information contained in this schematic is subject to change without notice. Chrontel Inc. bears no responsibility for any errors in this schematic.

Assembly Instructions:

"ellipse"



NOTE: Contents within the "ellipse" are NOT STUFFED! It is used only as options.

Do not stuff following items :

1) Sheet 3 of 8:

- R18, R19, R27, R52, R53, R102, R108, R111, R112, R113, R114, R115, R117

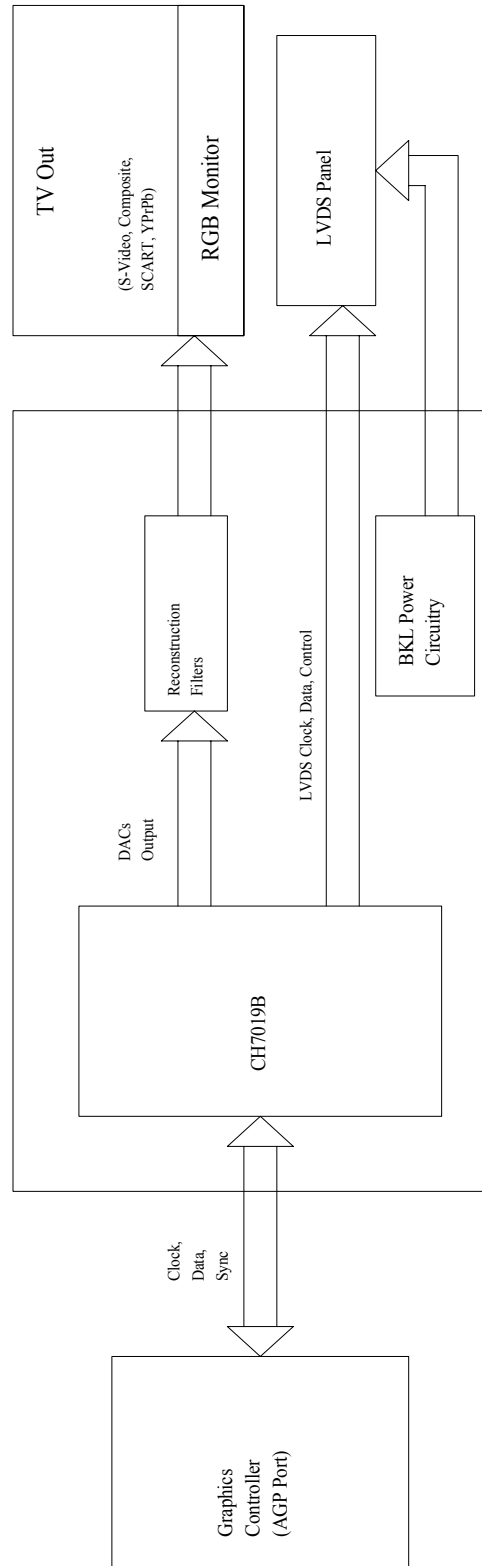
2) Sheet 4 of 8:

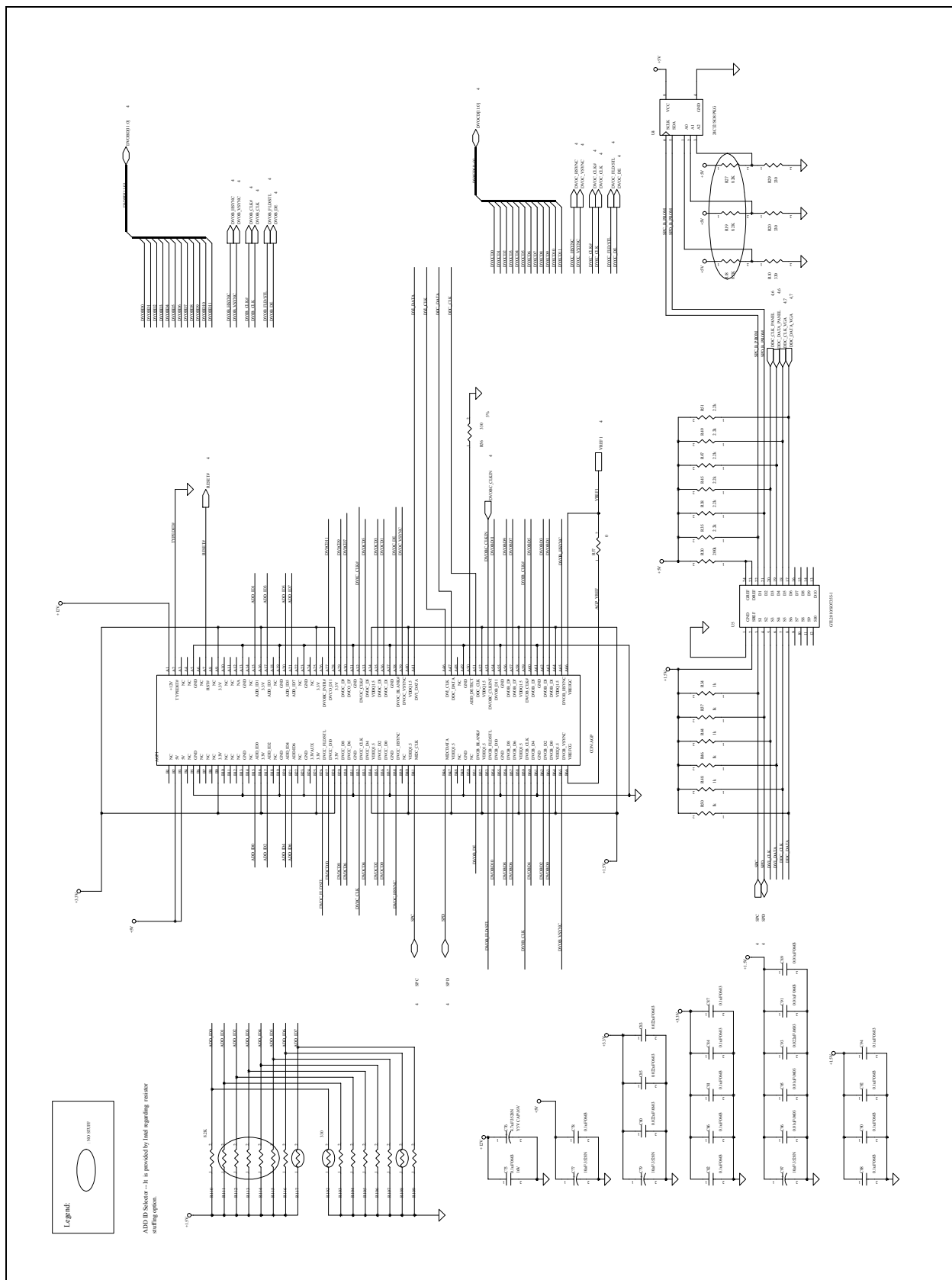
- JP3, R11, R12, R21, R22, R23, R24, R39, R40, R41, R42, R43, R65, R68, R70, R71, R72, R73, R74, R77, R78, R80, R94, R95, R96, R97, R99, R100

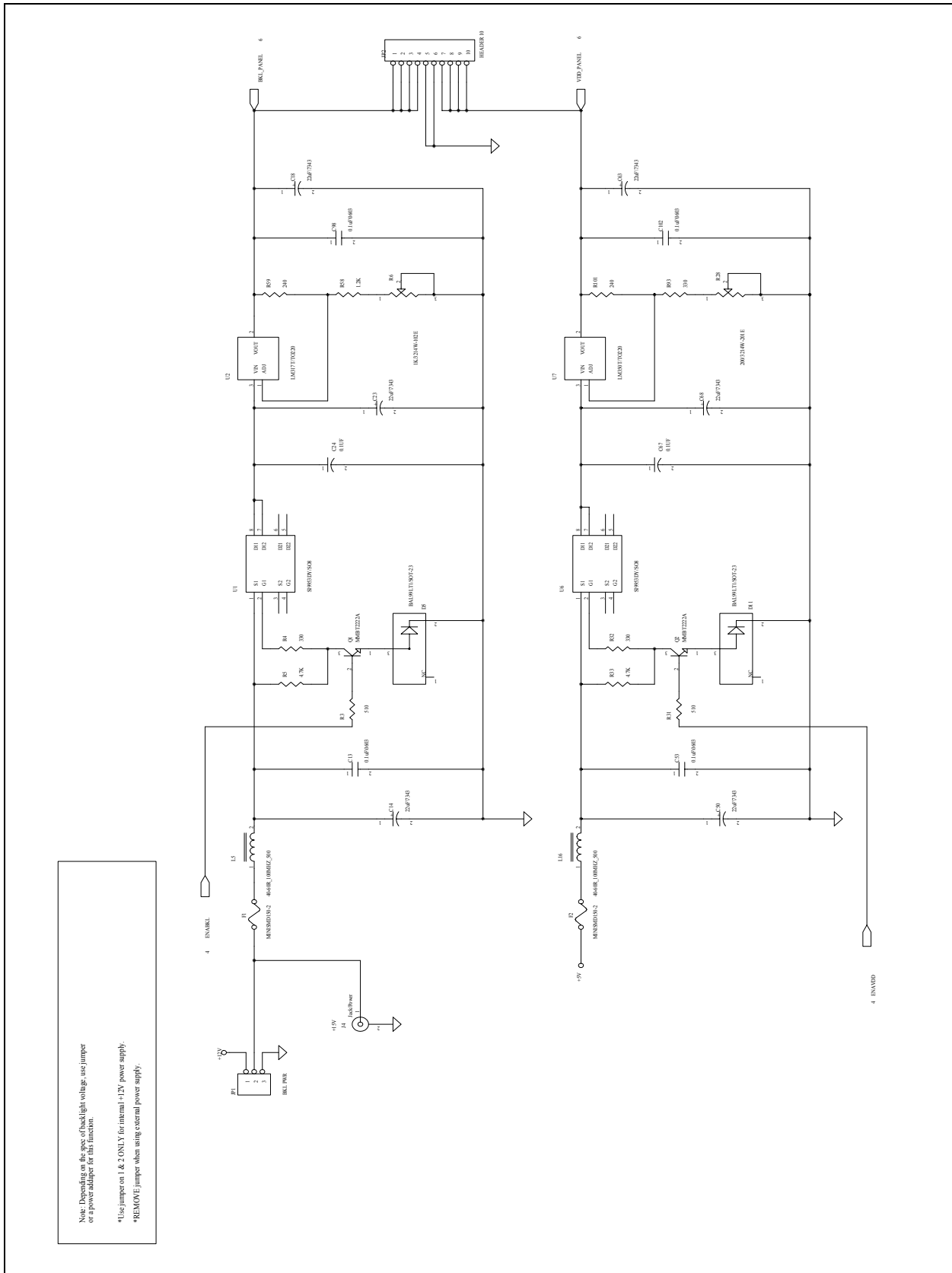
3) Sheet 7 of 8:

- R7, R16, R25, R36

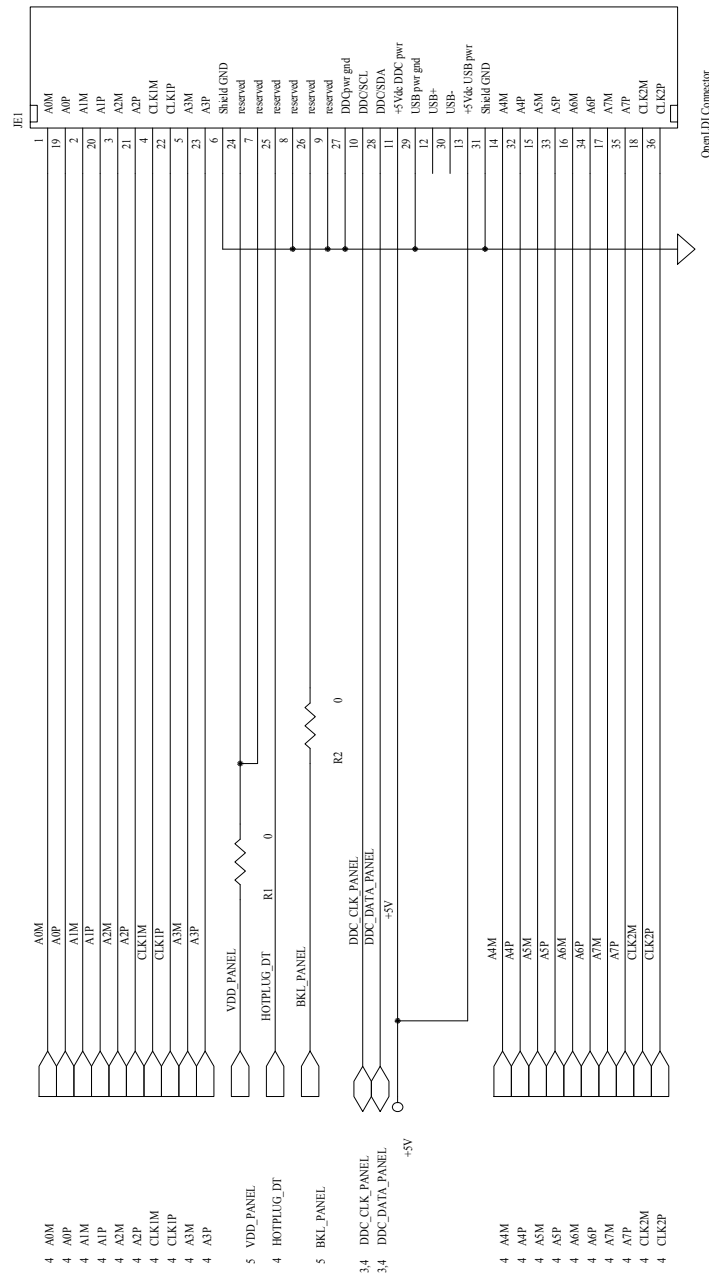
CH7019B Input_ Output Block Diagram

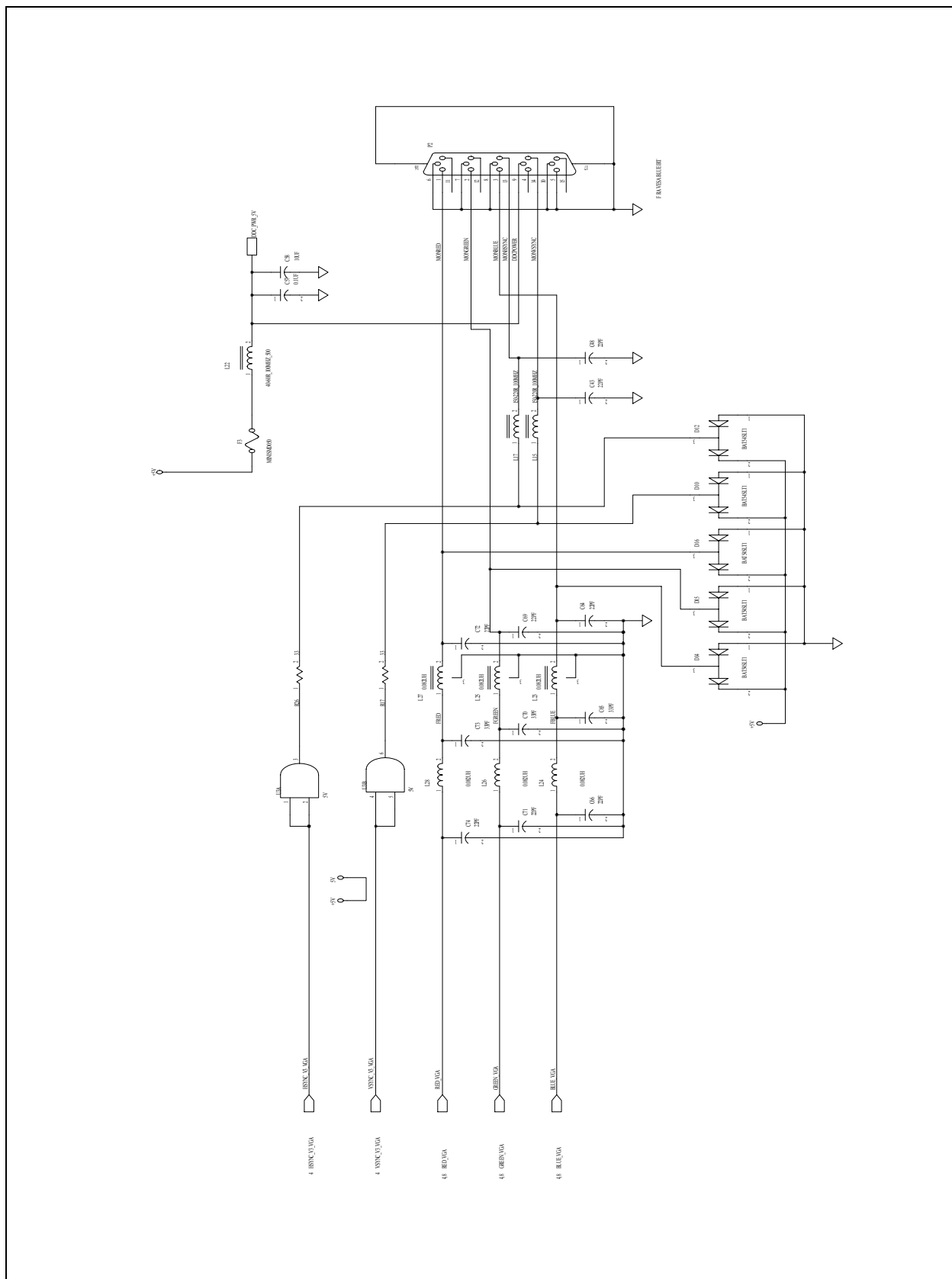




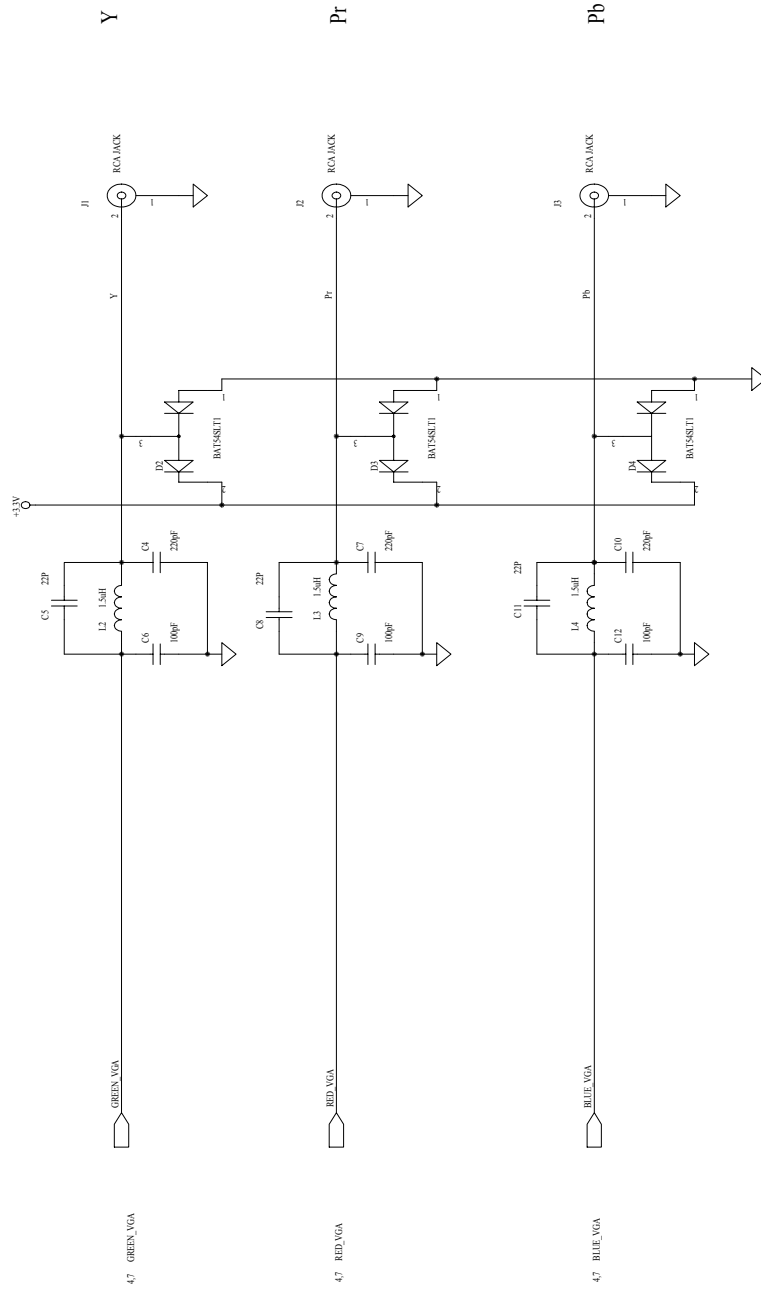


Open LDI Connector





TV Out YPrPb Mode



1. Revision History

Revision	Date	Section	Description
1.0	10/21/03	All	First official release, Revision 1.0

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