

PCB Layout and Design Considerations for the CH7021/CH7022 SDVO+SDTV/HDTV Encoder

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7021/CH7022 SDTV/HDTV Output Device with SDVO inputs. SDVO is a digital video interface developed by Intel. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for the SDTV/HDTV link are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production. CH7022 is almost the same chip as CH7021. The only difference is that CH7021 contains Macrovision encoding and CH7022 does not. Both chips share the same PCB design guide.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP and QFN package of the CH7021/CH7022. Please refer to the CH7021/CH7022 datasheet for the details of the pin assignments.

2. Component Placement and Design Considerations

Components associated with the CH7021/CH7022 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1 μ F ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11 and C12) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7021/CH7022 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7021/CH7022 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7021/CH7022 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate Digital, DAC, Analog, and TV PLL power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment of the CH7021/CH7022

Pin Assignment	# of Pins	Type	Symbol	Description
6, 13, 35	3	Power	DVDD	Digital Supply Voltage (2.5V)
9, 10, 37	3	Power	DGND	Digital Ground
16	1	Power	VDAC2	DAC Supply Voltage (3.3V)
17	1	Power	GDAC2	DAC Ground
19	1	Power	VDAC1	DAC Supply Voltage (3.3V)
23	1	Power	GDAC1	DAC Ground
27	1	Power	VDAC0	DAC Supply Voltage (3.3V)
31	1	Power	GDAC0	DAC Ground
41	1	Power	AVDD_TVPLL1	TV PLL1 Supply Voltage (2.5V)
38	1	Power	AGND_TVPLL1	TV PLL1 Ground
42	1	Power	AVDD_TVPLL2	TV PLL2 Supply Voltage (2.5V)
45	1	Power	AGND_TVPLL2	TV PLL2 Ground
52, 58, 64	3	Power	AVDD	Analog Supply Voltage (2.5V)
49, 55, 61	3	Power	AGND	Analog Ground
33	1	Power	V5V	D-Connector Supply Voltage (5V)

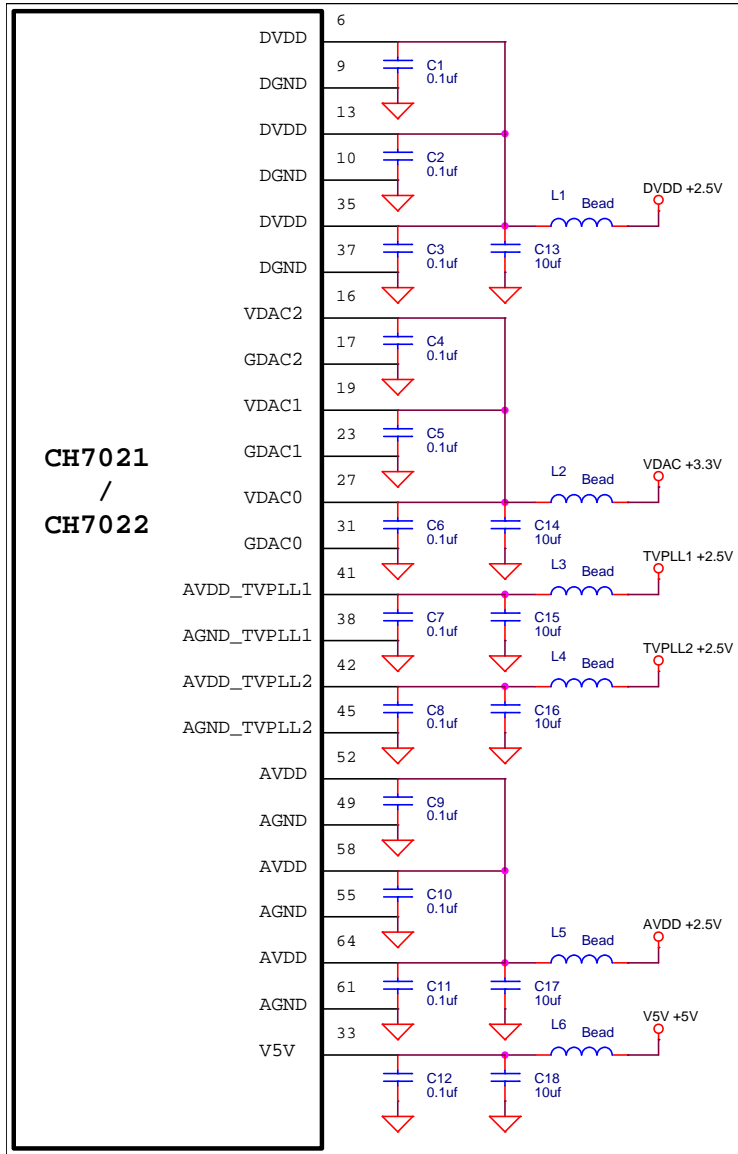


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

2.2 General Control and SDVO Signals

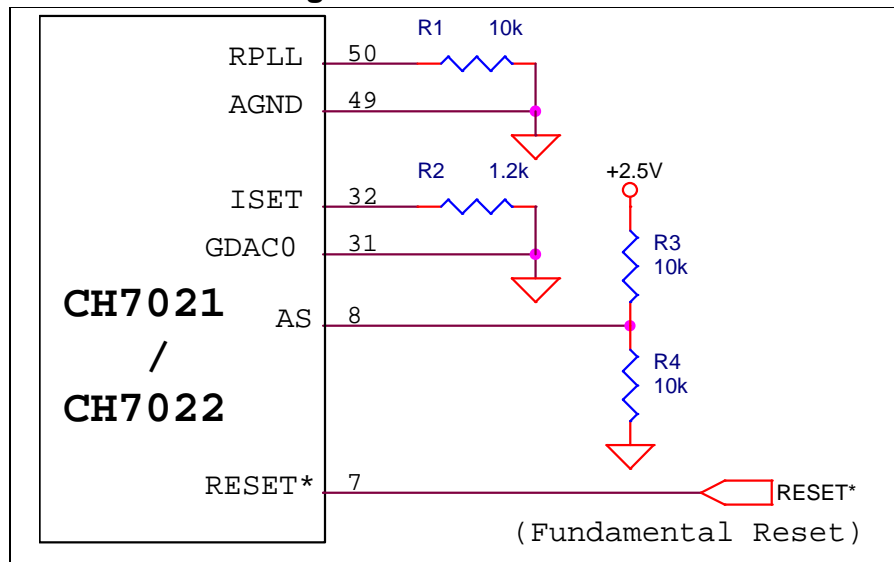


Figure 2: ISET, AS, RPLL and RESET* pin connection

- **ISET pin**

A 1.2kΩ resistor should be connected directly between ISET (pin 32) and DAC ground (pin 31) and as close as possible to the ISET pin using short and wide traces. See **Figure 2** for design reference.

- **AS pin**

The Address Select pin, pin 8, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled ‘low’, then the serial port address is 72h. If AS is pulled ‘high’, then the serial port address is 70h.

- **RPLL pin**

A 10kΩ resistor should be connected directly between RPLL (pin 50) and AGND (pin 49) and as close as possible to the RPLL pin using short and wide traces. See **Figure 2** for design reference.

- **RESET* pin**

The RESET* pin should be connected to the Fundamental Reset of the GMCH as shown in **Figure 2**. When this pin is pulled ‘low’, the device is held in the power-on reset condition. When this pin is high, the reset of the device is controlled through the serial port.

- **Serial Video Inputs**

(SDVO_CLK-, SDVO_CLK+, SDVO_R-, SDVO_R+, SDVO_G-, SDVO_G+, SDVO_B-, SDVO_B+)

Since the digital serial data of the CH7021/CH7022 may toggle at speeds up to 2Gb/s (depending on input clock speed), it is strongly recommended that the connection of these video signals between the graphics controller and the CH7021/CH7022 be kept short (maximum 4 inches from edge finger to the CH7021/CH7022) and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mil traces be used in routing these signals. There should be 7 mil spacing between each intra pair (e.g. Red+ to Red-). Spacing between inter pairs (e.g. Red to Green) should be 20 mils. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bends greater than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH.

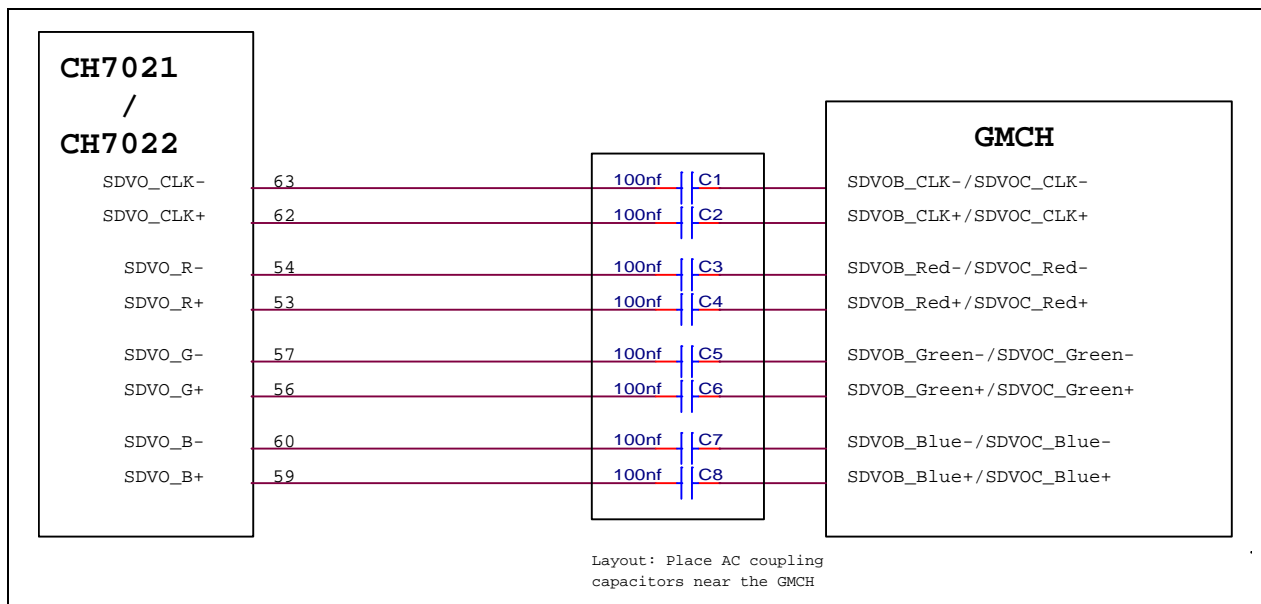


Figure 3: Differential serial video inputs

- **TVCLK-, TVCLK+**

TVCLK-, TVCLK+ are differential outputs from the CH7021/CH7022. This pair outputs a differential clock to the GMCH. The GMCH uses this as a reference frequency to generate SDVO_CLK+/- sending to CH7021/CH7022. 100nF capacitors should be placed close to the CH7021/CH7022 as AC coupling capacitors (See **Figure 4**).

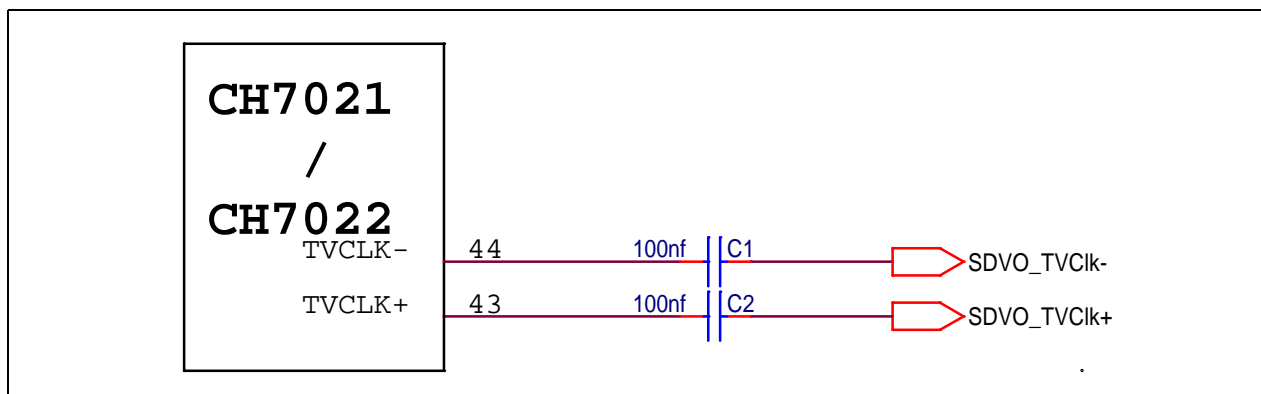


Figure 4: TVCLK+/- differential pair AC coupling capacitors

2.3 Serial Port Interface

- **SPD and SPC pins**

SPD (pin 11) and SPC (pin 12) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 5.6 KΩ resistors (See **Figure 5**).

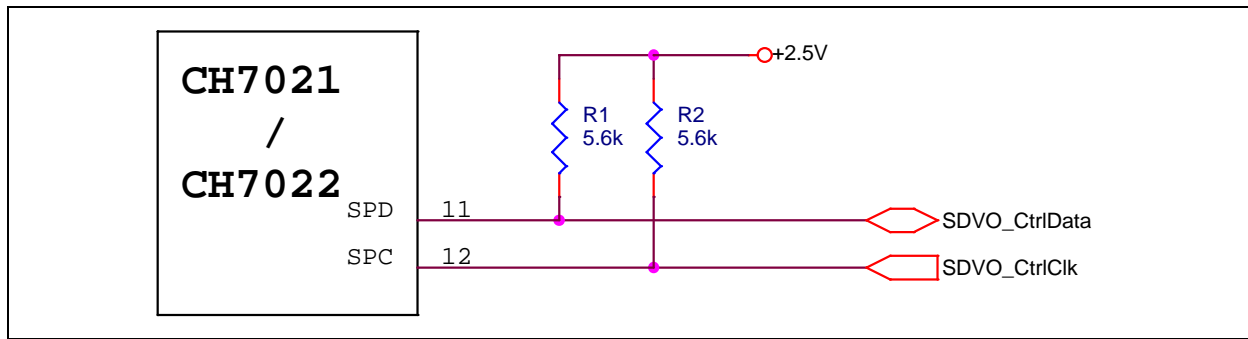


Figure 5: Serial Port Interface: SPD and SPC pins

• **SD_PROM and SC_PROM**

SD_PROM (pin 4) and SC_PROM (pin 5) are used to interface with the serial PROM on the ADD2[†] card. In the reference design, SD_PROM and SC_PROM are pulled up with 5.6 K Ω resistors (See Figure 6). If the design is on the motherboard-down, the PROM is not required and both SD_PROM and SC_PROM can be either pulled up or floating.

[†] Note: ADD2 Card: Advanced Digital Display Card - 2nd Generation. It provides digital display options for an Intel[®] graphics controller that supports the SDVO interface. It will not work with the graphics controller that supports Intel[®] DVO interface.

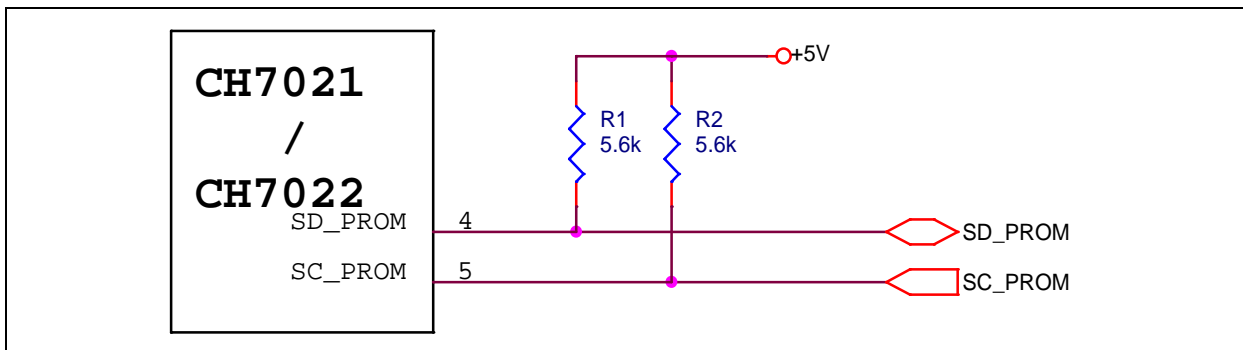


Figure 6: Serial Port Interface: SD_PROM and SC_PROM pins

• **SD_DDC and SC_DDC**

SD_DDC (pin 2) and SC_DDC (pin 3) are used to interface with the RGB monitor's DDC. In the reference design, SD_DDC and SC_DDC are pulled up with 10 K Ω resistors to 5V. (See Figure 7).

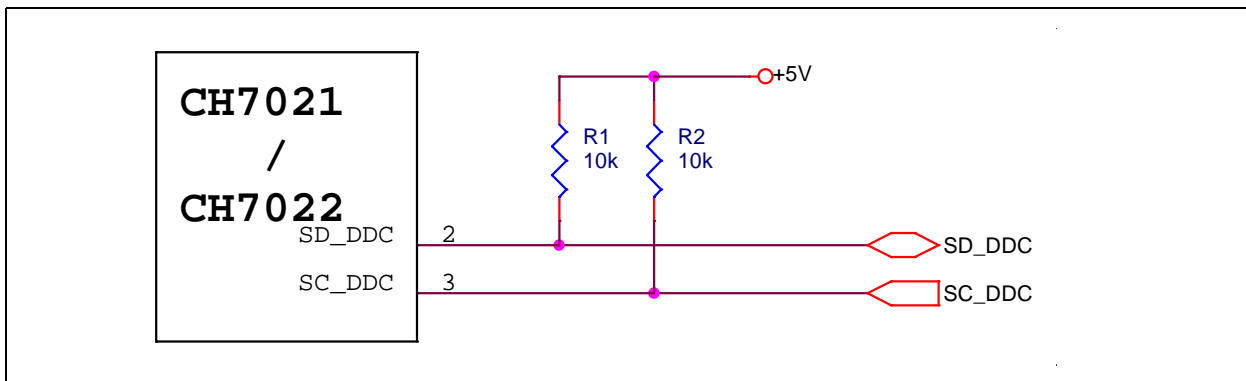


Figure 7: Serial Port Interface: SD_DDC and SC_DDC pins

2.4 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

The XI/FIN and XO pins are used for reference input clock to the CH7021/CH7022. The CH7021/CH7022 can accept a 27MHz crystal (+/- 20ppm). An external CMOS compatible clock can also drive the XI/FIN input of the CH7021/CH7022. For PCB design, the crystal must be placed as close as possible to the XI/FIN and XO pins (Pins 39 and 40), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7021/CH7022, it is very important that noise should not couple into these input pins. Decoupling capacitors should be added to both sides of the crystal to ensure the accuracy of the input frequency to the CH7021/CH7022 device. Traces with fast edge rates should not be routed under or adjacent to these pins. Please see **Figure 8** for details.

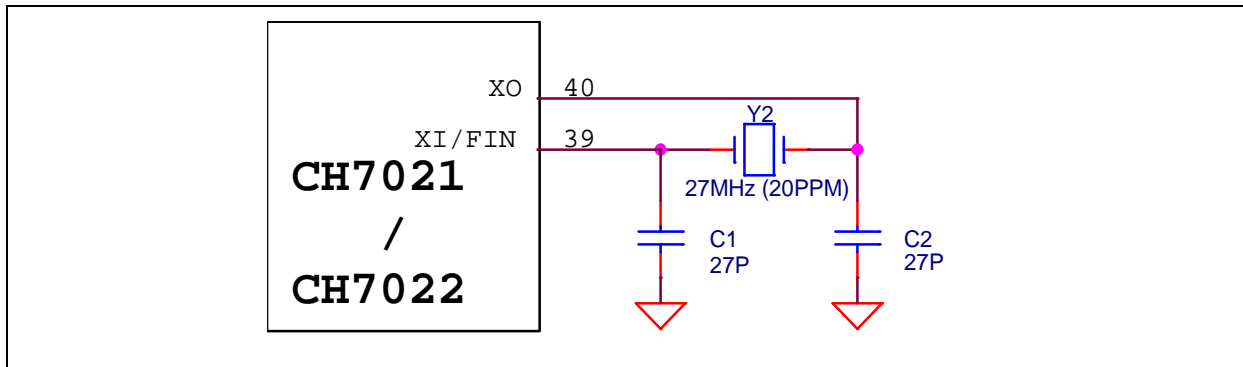


Figure 8: Crystal Oscillator Connection

- **Reference Crystal Oscillator**

The CH7021/CH7022 includes an oscillator circuit that allows a 27MHz crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to the CH7021/CH7022. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be 27MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to the CH7021/CH7022 (C_{ext}).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$$

where:

C_{ext} = external load capacitance required on XI/FIN and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7021/CH7022 (approximately 10-15 pF on each of XI/FIN and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,

$$C_{int\ XI/FIN} = C_{int\ XO} = C_{int}$$

$$C_{ext\ XI/FIN} = C_{ext\ XO} = C_{ext}$$

such that

$$C_L = (C_{int} + C_{ext}) / 2 + C_S \quad \text{and} \quad C_{ext} = 2(C_L - C_S) - C_{int}$$

$$= 2C_L - (2C_S + C_{int})$$

Therefore C_L must be specified greater than $C_{int} / 2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.5 Miscellaneous Pins

- **CHSYNC and VSYNC Pins**

CHSYNC is the composite or horizontal sync output pin. A buffered version of VGA horizontal sync can be acquired from this pin.

VSYNC is the vertical sync output pin. A buffered version of VGA vertical sync can be acquired from this pin (See **Figure 9**). **Figure 10** shows a paradigm of VGA RGB monitor connection in which CHSYNC and VSYNC are involved.

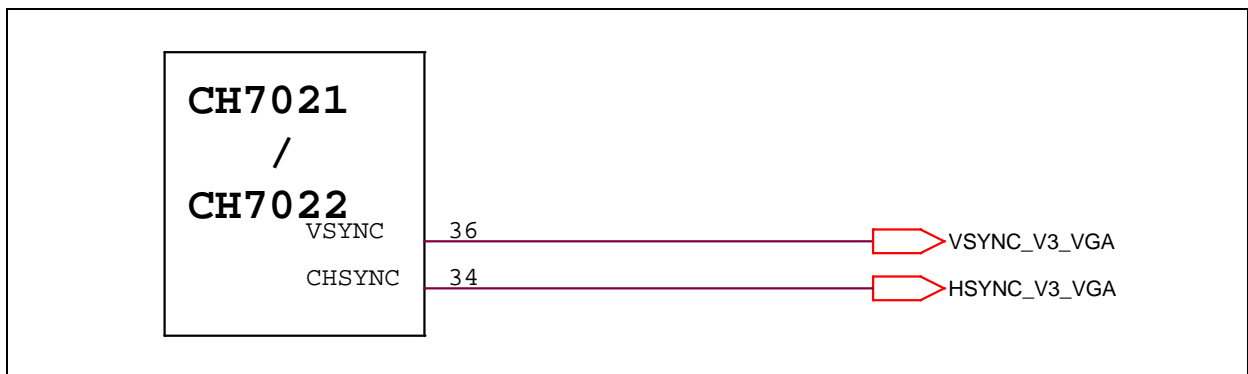


Figure 9: VSYNC and CHSYNC Connection

- **T1, T2, BSCAN and Reserved Pins**

T1 and T2 pins are used for internal test purpose only. These pins should be left open in the application.

BSCAN and Reserved pins are used for internal test purpose only. These pins should be left open or pulled low with a 10kΩ resistor in the application.

2.6 Analog RGB Output

Table 2 shows the video out connectors from the DACs of CH7021/CH7022.

Table 2: Video DAC Configuration

Output Type	DACA[0]	DACA[1]	DACA[2]	DACA[3]
SCART	B	G	R	CVBS
CRT	B	G	R	
	DACB[0]	DACB[1]	DACB[2]	
S-Video		Y	C	
CVBS	CVBS			
	DACC[0]	DACC[1]	DACC[2]	
YPrPb	Pb	Y	Pr	

The R, G, B (pins 20, 24, and 28) signals are analog video signals. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the R, G, B signals and 20 mils spacing between them and any digital trace.

Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corners should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them. See Figure 10 for CRT RGB monitor connection.

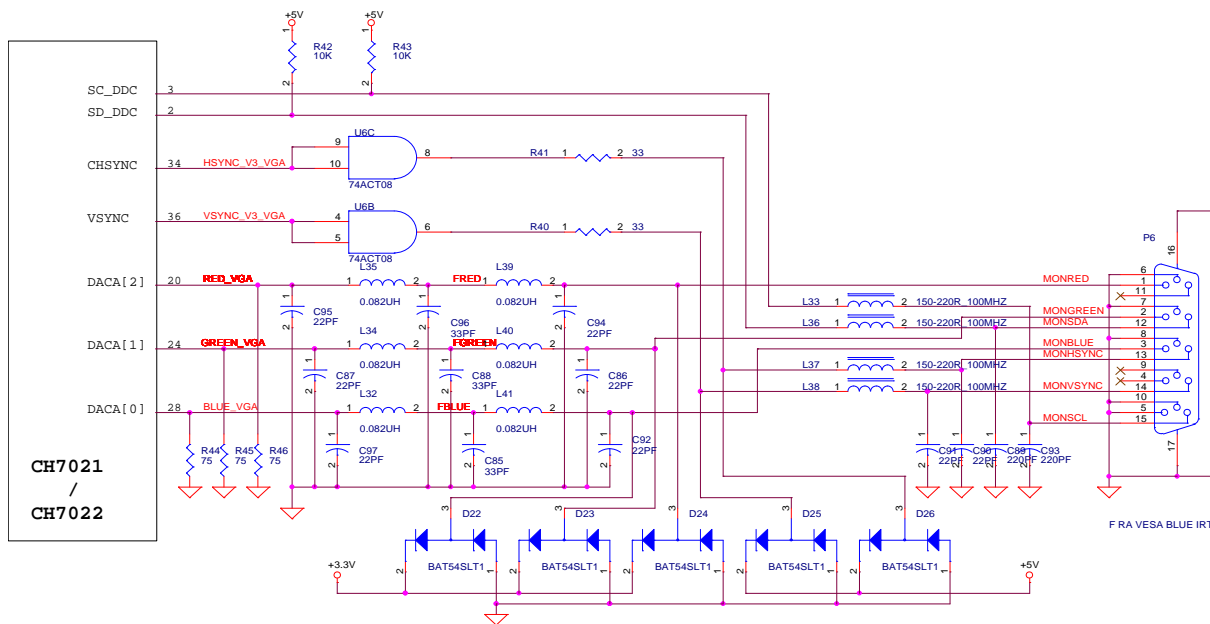


Figure 10: CRT RGB Monitor Connection

2.7 TV Output and Control

The components associated with the video output pins should be placed as close as possible to the CH7021/CH7022. The 75Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7021/CH7022 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs or Y, Pr and Pb signals should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit for a muxing HDTV/S-Video and composite outputs are shown in **Figure 11**. **Figure 12** shows a 7-pin Mini DIN connector muxing output HDTV/S-Video/CVBS. For muxing output, no more than one output connected to the 7-pin connector at the same time is allowed.

In case, CRT RGB and SCART RGB outputs are both required, the reconstruction filter for CRT RGB should be implemented. Please refer to the reference schematics at the end of this document for SCART RGB out, which share the reconstruction filter network with CRT RGB out.

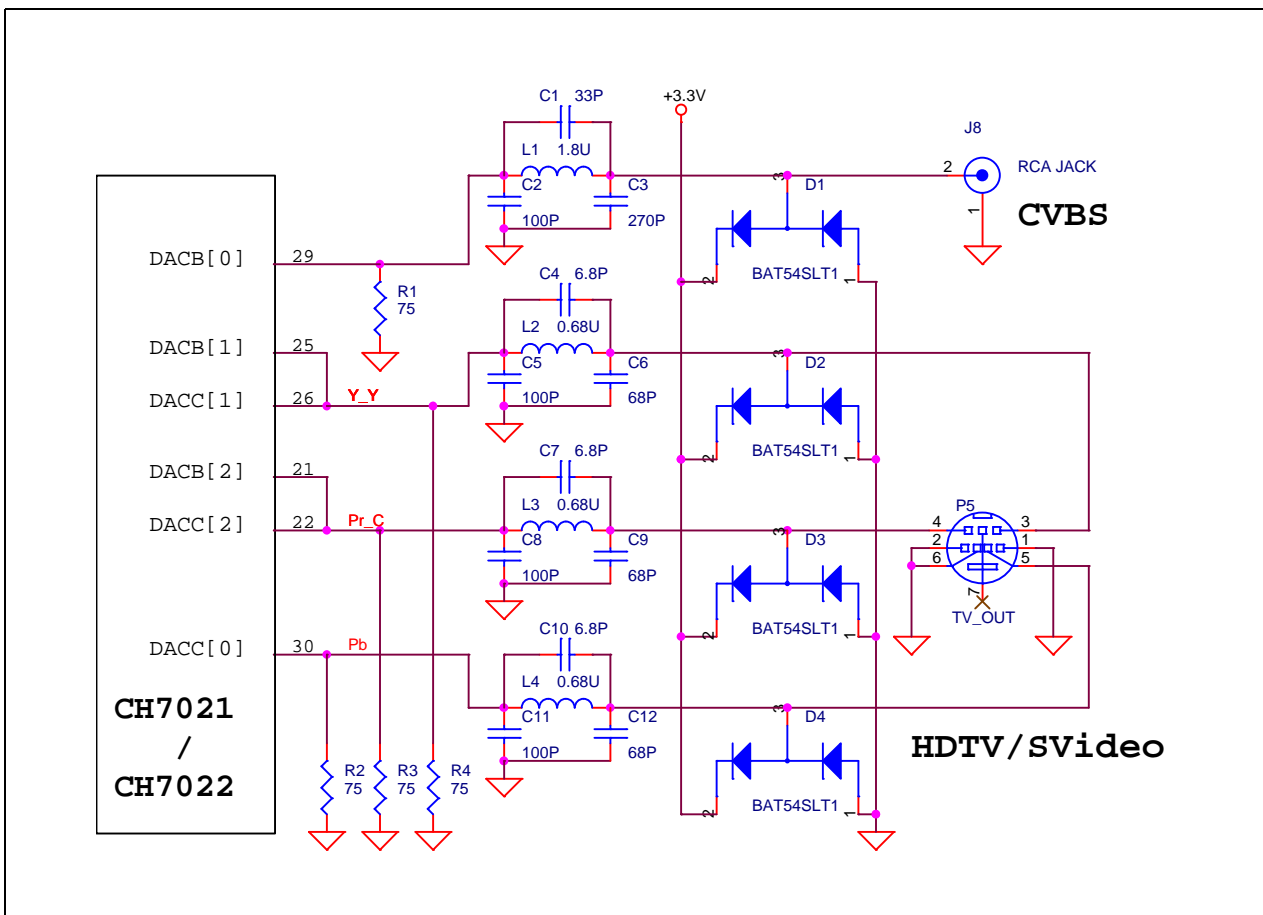


Figure 11: The Connection for the muxing HDTV/S-Video and Composite Outputs

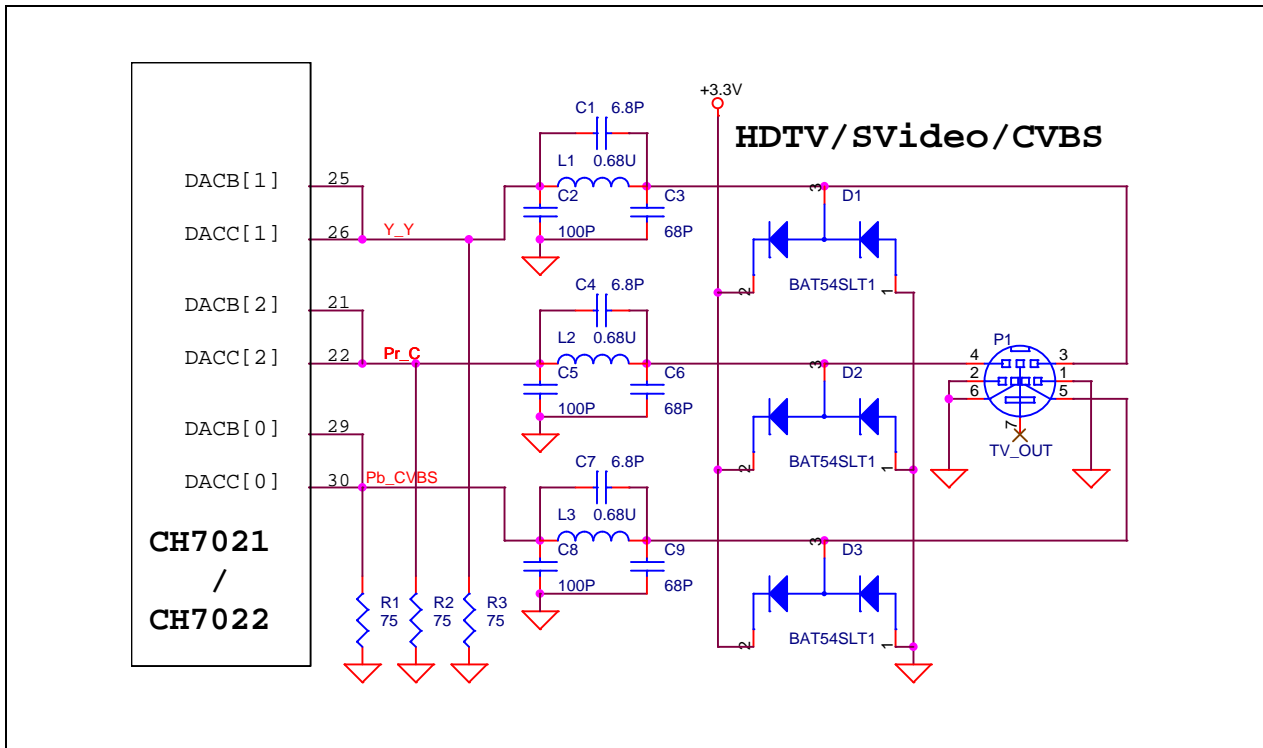


Figure 12: Muxing connection for HDTV/S-Video/CVBS

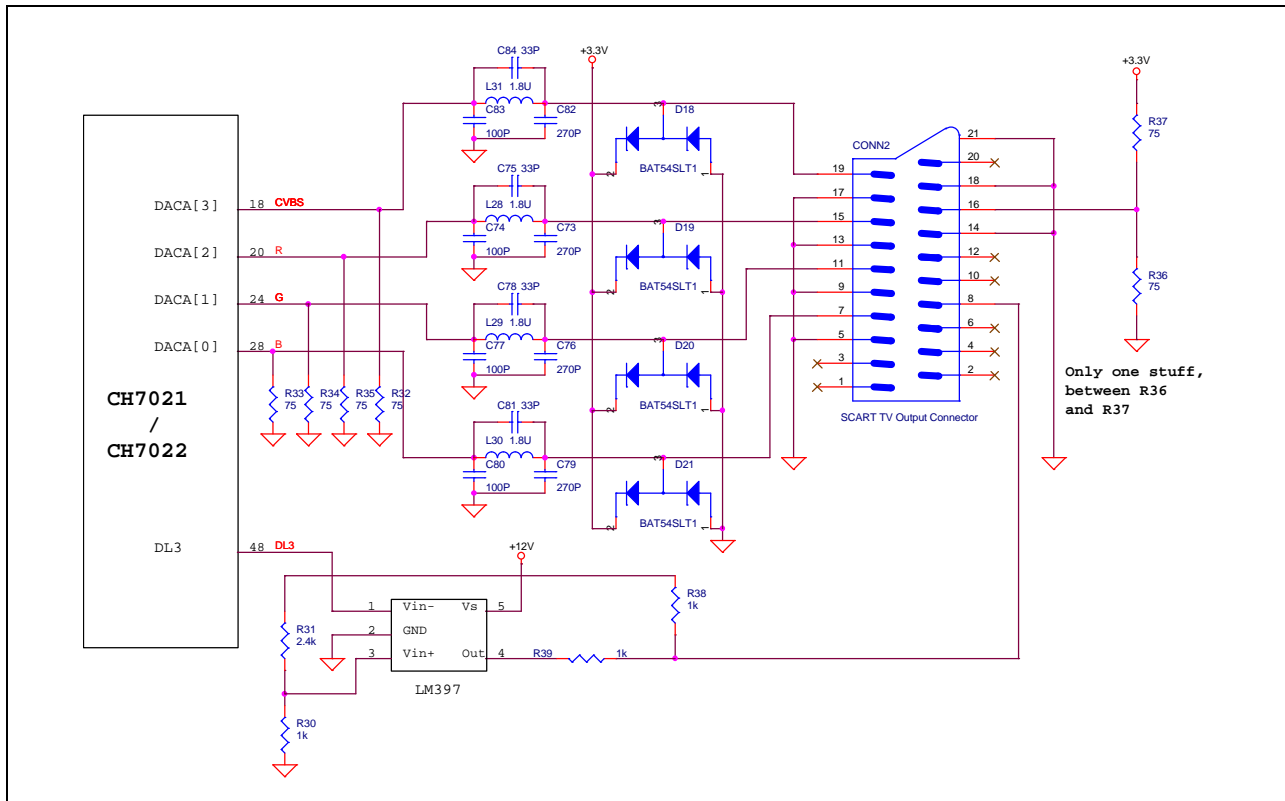


Figure 13: The Connection for the SCART Connector

Figure 13 shows the connection for the SCART output.

Pin 8 on the SCART connector can be used to signal the SCART monitor to change the display aspect ratio. Using the circuit shown above:

When DL3 = 0V, SCART Pin 8 = ~12V. SCART monitor should be displaying a 4:3 aspect ratio.

When DL3 = 5V, SCART Pin 8 = ~6.5V. SCART monitor should be displaying a 16:9 aspect ratio.

Note that the CH7021/CH7022 is always outputting SCART in 4:3 aspect ratio, it is up to the SCART monitor to resize when necessary.

Pin 16 on the SCART connector can be used to signal the SCART monitor to display either in CVBS mode or in RGB mode. This pin receives power from the board.

When Pin 16 = 0 to 0.4V, the SCART monitor will accept CVBS input only.

When Pin 16 = 1 to 3V, the SCART monitor will accept CVBS + RGB input.

In the circuit shown above, SCART connector pin 16 can be either tied high or low using jumper selection.

In case, VGA RGB and SCART RGB outputs are both required, the reconstruction filter for VGA RGB should be implemented. Please refer to the reference schematics at the end of this document for SCART RGB out, which share the reconstruction filter network with VGA RGB out.

2.8 HDTV Output and Control

Careful layout consideration for the Y, Pr, Pb traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, Pr, Pb be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

Figure 11 shows the muxing connection for the HDTV and S-Video using 7-pin mini connector. **Figure 14** shows the separated connection for the HDTV/YPrPb. And **Figure 15** shows the connection for the HDTV D-Connector.

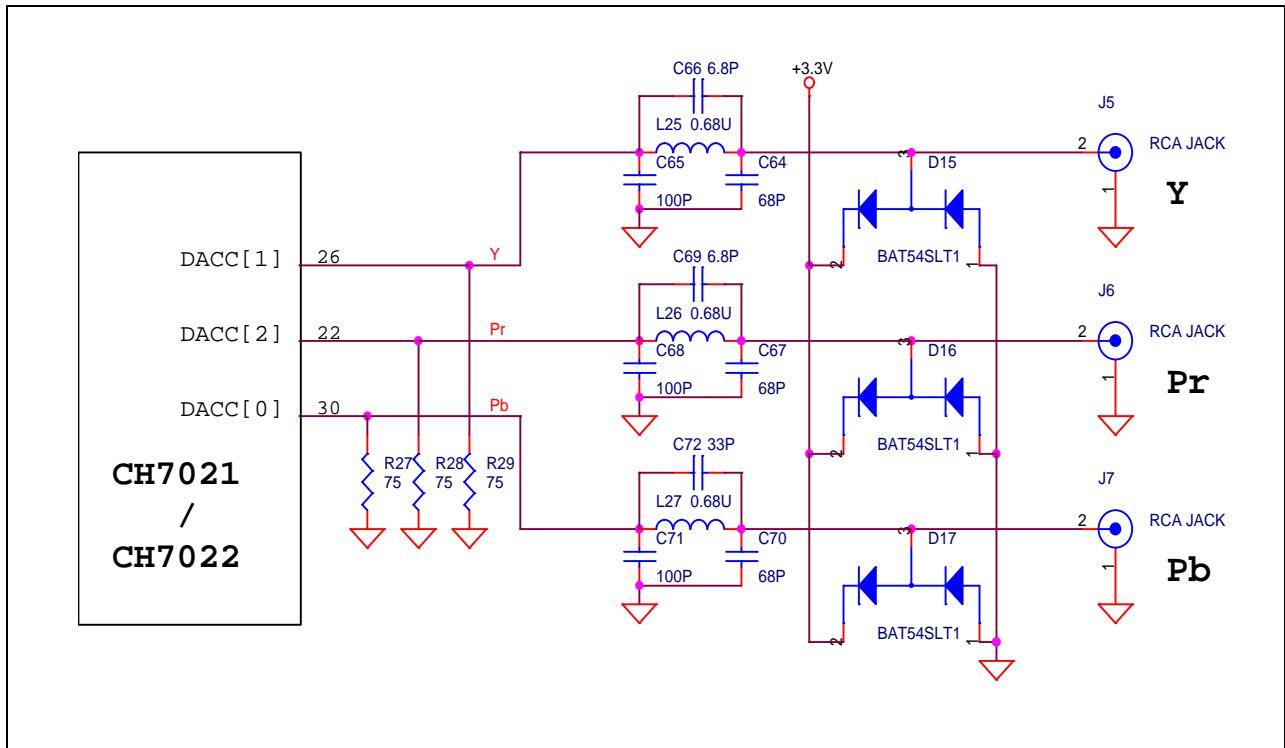


Figure 14: The Connection for HDTV/YPrPb

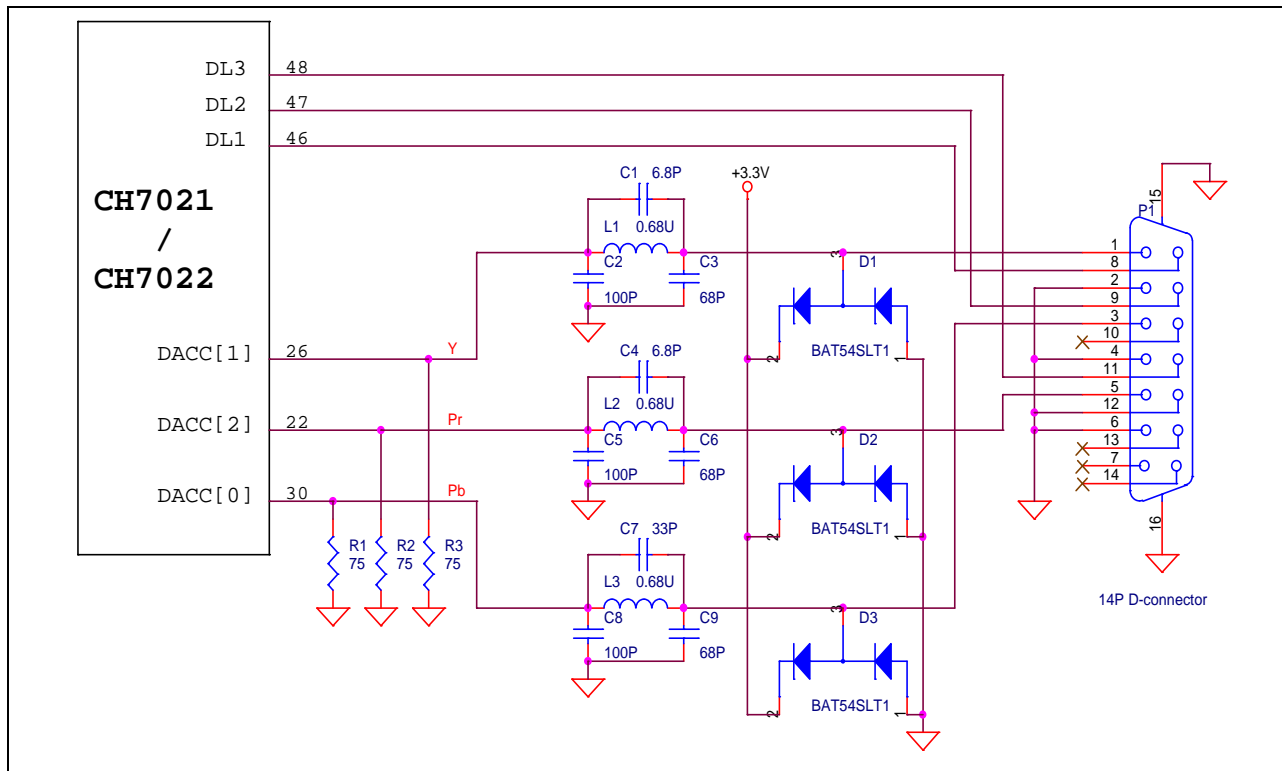


Figure 15: The Connection for the HDTV D-Connector

2.9 64 Pin LQFP and QFN with Thermal Exposed Pad Package

The CH7021/CH7022 is available in a 64 pin LQFP and QFN with thermal exposed pad package. The part numbers are CH7021/CH7022-TEF and CH7021/CH7022-BF, respectively. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7021/CH7022.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 16**.

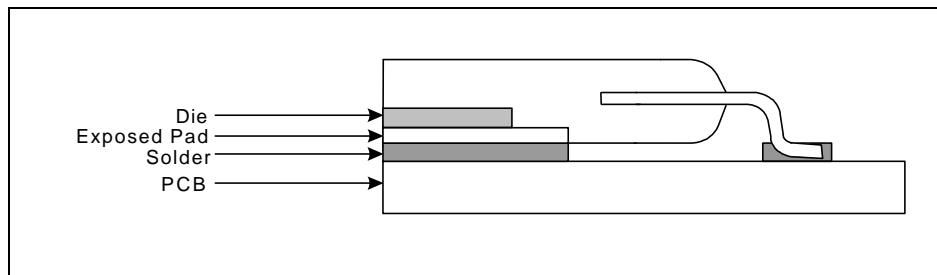


Figure 16: Cross-section of the LQFP and QFN exposed pad package

We should attend the placement of the thermal land pattern. Thermal pad dimension is from 5.85mm to 7mm (min to max), 5.85mm x 5.85mm is the minimum size recommended for the thermal pad, and 7mm x 7mm is the maximum size. The thermal land pattern should have a 3x3 grid array of 2mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.38mm in diameter with 1 oz copper via barrel plating. You can see it in **Figure 17**.

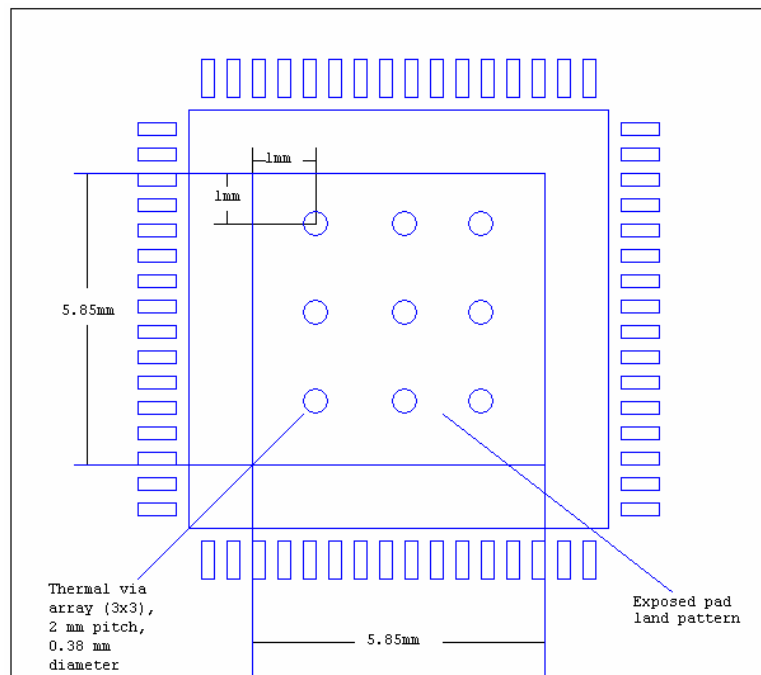


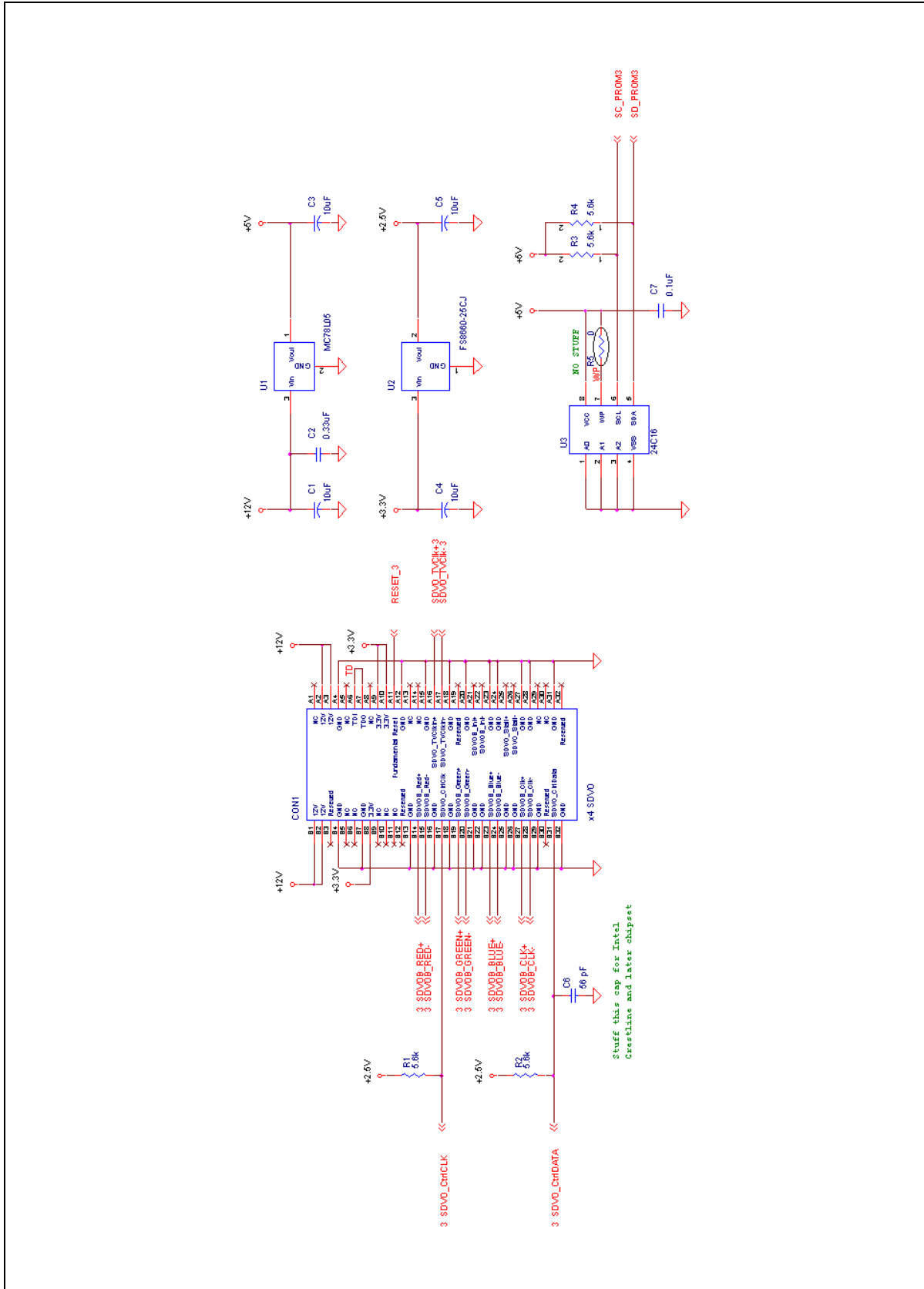
Figure 17: Thermal Land Pattern

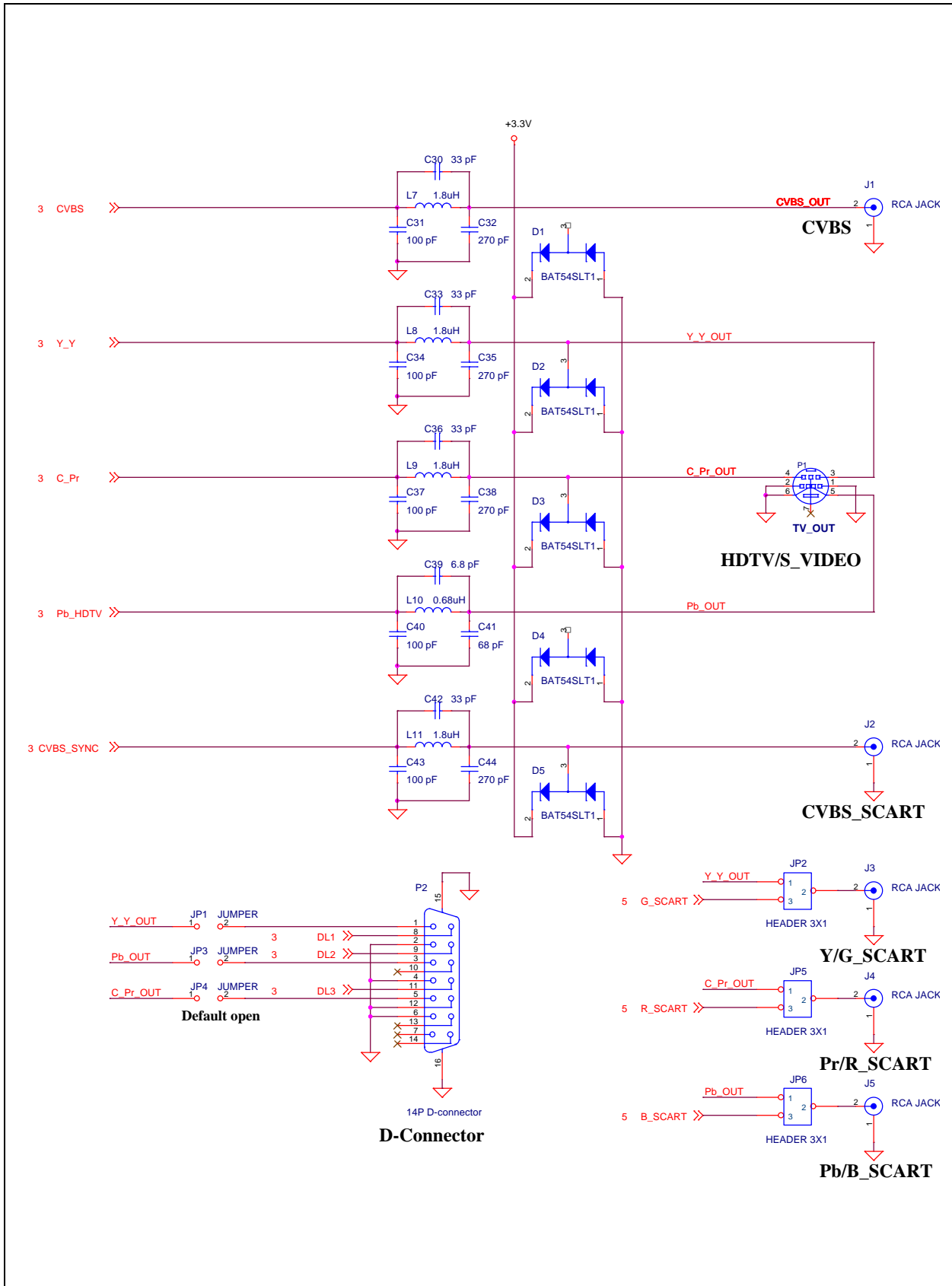
When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. Thermal resistance was calculated using the thermal simulation program called ANSYS.

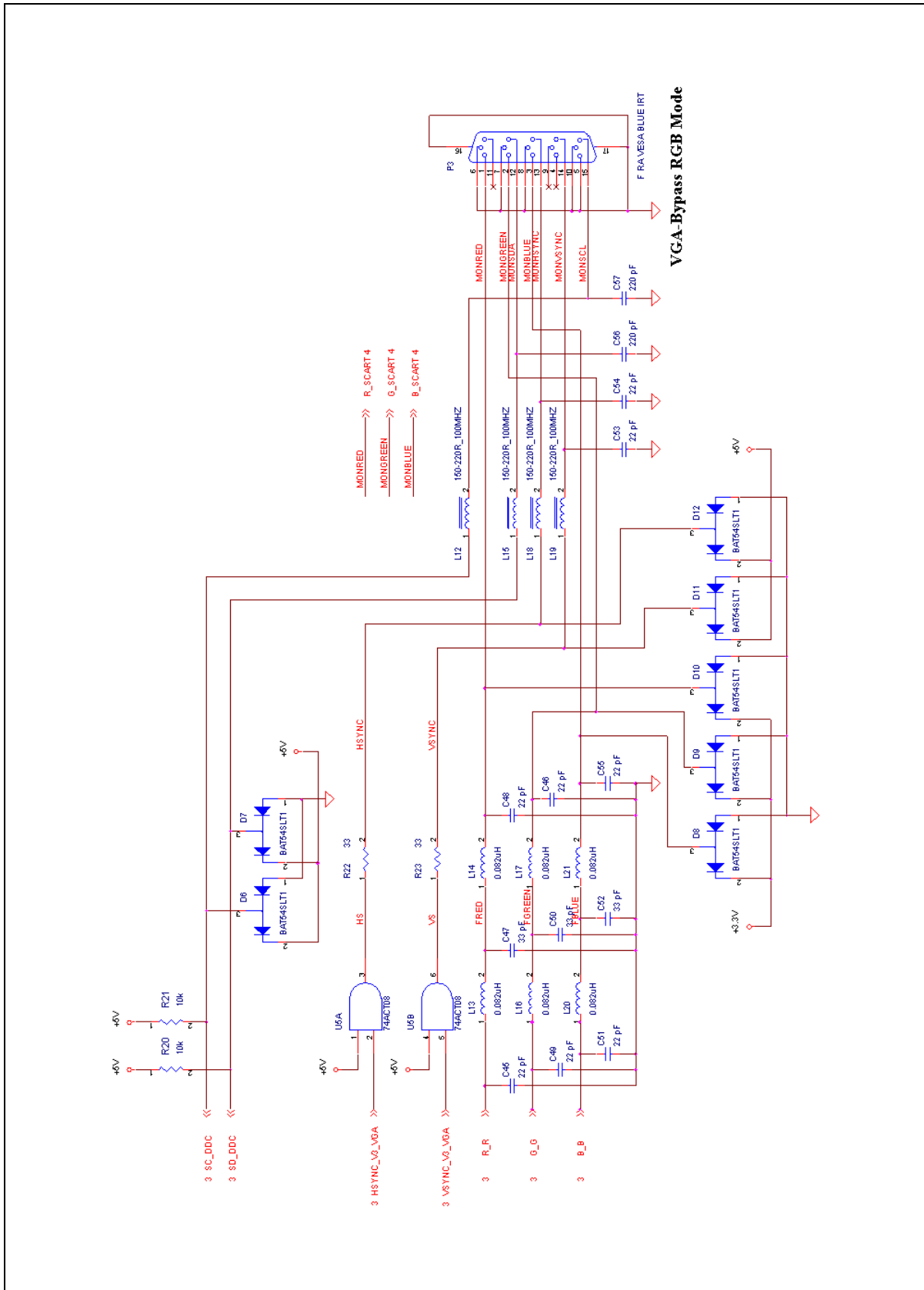
3. Reference Design Example

The following schematics are based on an Intel[®] SDVO graphics chipset design and are to be used as a CH7021/CH7022 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7021/CH7022 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example







3.2 Evaluation Board Preliminary BOM

Item	Quantity	Reference	Part
1	1	CON1	x4 SDVO
2	10	C1,C3,C4,C5,C8,C17,C19, C20,C25,C29	10uF
3	1	C2	0.33uF
4	1	C6	56 pF
5	15	C7,C9,C10,C11,C14,C15, C16,C18,C21,C22,C23,C24, C26,C27,C28	0.1uF
6	2	C12,C13	27 pF
7	7	C30,C33,C36,C42,C47,C50, C52	33 pF
8	5	C31,C34,C37,C40,C43	100 pF
9	4	C32,C35,C38,C44	270 pF
10	1	C39	6.8 pF
11	1	C41	68 pF
12	8	C45,C46,C48,C49,C51,C53, C54,C55	22 pF
13	2	C56,C57	220 pF
14	12	D1,D2,D3,D4,D5,D6,D7,D8, D9,D10,D11,D12	BAT54SLT1
15	3	JP1,JP3,JP4	JUMPER
16	3	JP2,JP5,JP6	HEADER 3X1
17	5	J1,J2,J3,J4,J5	RCA JACK
18	6	L1,L2,L3,L4,L5,L6	Bead
19	4	L7,L8,L9,L11	1.8uH
20	1	L10	0.68uH
21	4	L12,L15,L18,L19	150-220R_100MHZ
22	6	L13,L14,L16,L17,L20,L21	0.082uH
23	1	P1	TV_OUT
24	1	P2	14P D-connector
25	1	P3	F RA VESA BLUE IRT
26	4	R1,R2,R3,R4	5.6k
27	1	R5	0
28	7	R6,R7,R8,R9,R10,R20,R21	10k
29	8	R11,R12,R13,R14,R15,R16, R17,R18	75
30	1	R19	1.2K
31	2	R22,R23	33
32	1	U1	MC78L05
33	1	U2	FS8660-25CJ
34	1	U3	24C16
35	1	U4	CH7021/CH7022
36	1	U5	74ACT08
37	1	Y1	HCM49-27MHz

4. Revision History

Revision	Date	Section	Description
0.9	07/21/04	All	First draft release, revision 0.9
0.91	10/20/04	2.8	Add S-Video/CVBS/HDTV 7-pin mux.
0.92	01/06/04	2.6	Remove whole 2.6 for exposed pad description
0.93	01/25/04	2.7	Add notes for SCART connector.
0.94	09/28/05	Fig. 13	Add voltage inverter and description
0.95	10/06/05	Fig. 13	Update drawing with input control and description.
1.0	12/4/05	2.9	Add 64 Pin LQFP and QFN with Thermal Exposed Pad Package.
1.1	3/30/07	Fig.14 & 15	Corrected the value of C7 to 6.8pF on Figure 14 and Figure 15 .
1.2	10/16/07	All	Add QFN package, add a 56 pF to GND on trace SDVO_CtrlDATA and add EMI protect diode on SC_DDC and SD_DDC.
2.0	03/27/08	All	Combined CH7021 and CH7022
2.1	06/20/08	1, 2.2, 2.3, 2.9, 3, Fig.13	Make some expression more accurate and schematic more clear. Modify Fig.13 SCART connection.
2.11	01/20/2009	Fig. 10	Change 74ACT00 to 74ACT08

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