
CH7023 Registers Read/Write Operation

1. Introduction

The Chrontel CH7023 contains a serial port interface, through which the control registers can be written to and read from. The serial interface consists of SPD (bidirectional serial port data) and SPC (serial port clock).

The serial port clock line (SPC) is input only and is driven by the output buffer of the graphics controller device, which is the clock master in the system. The serial port data line (SPD) is either input to or output from the encoder depending on the write or read status. The data on the line can be transferred up to 400 kbits/s. **Figure 1** shows the connection of the serial port interface.

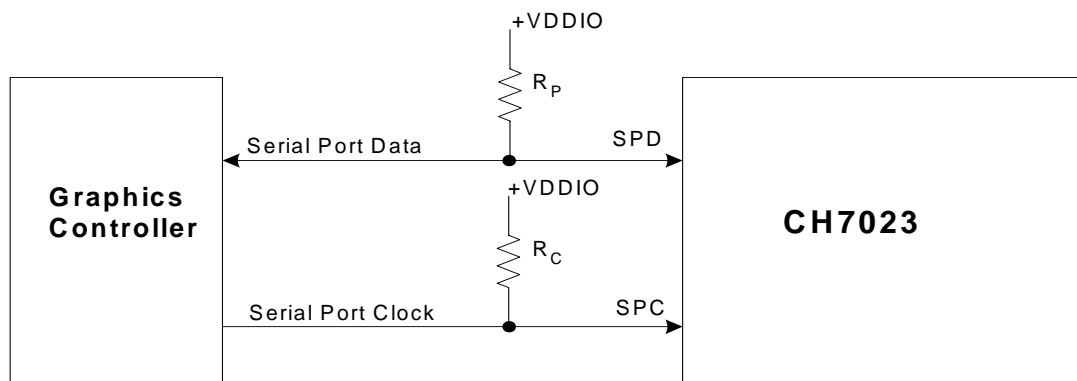


Figure 1: The Connection of the Serial Port Interface

2. Serial Port Operation

2.1 Electrical Characteristics of the Serial Port

The connections of the serial port interface is shown in **Figure 1**. A pull-up resistor (R_P) must be connected to the same voltage supply seen by the serial port interface pins. The serial port input voltage level is determined by VDDIO. A weak pull-up resistor (R_C) may be added to the clock line to ensure that it is pulled high when the line is free.

Maximum and minimum values of pull-up resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Line capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 2mA at $V_{OL_{max}} = 0.4$ V for the output stages:

$$R_P \geq (V_{DD} - 0.4) / 2 \quad (R_P \text{ in } k\Omega)$$

The line capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for R_P is shown below:

$$R_P \leq 10^3 / C \quad (\text{where: } R_P \text{ is in } k\Omega \text{ and } C, \text{ the total capacitance, is in } pF)$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μ A. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, the input current limits the maximum value of R_P . The R_P limit depends on V_{DD} and is shown below:

$$R_P \leq (100 \times V_{DD}) / I_{input} \quad (\text{where: } R_P \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A)$$

2.2 Transfer Protocol

Both read and write cycles can be executed in “Single-step”, or “Auto-increment”. Auto-increment read/write allows you to establish the initial register location, then automatically increments the register address after each subsequent data access so that the next register address does not need to be resent through the SPC/SPD serial interface lines. When Auto-increment is set, the initial address is first sent to the encoder then data1 is sent, then data2, then data3, and so forth. Single-step read/write, is a simplified version of the Auto-increment read/write with a single set of data instead of multiple data that is sent to or received from a specific register. The description of the transfer protocol is as follows:

The transfer sequence is initiated when a high-to-low transition of SPD occurs while SPC is high; this is the “START” condition. Transitions of address and data bits can only occur while SPC is low.

The transfer sequence is terminated when a low-to-high transition of SPD occurs while SPC is high; this is the “STOP” condition.

Upon receiving the first START condition, the Chronitel encoder expects a Device Address Byte (DAB) from the master device. The DAB data format is shown below. Bits B[7:1] of the DAB is referred to as the serial port address. When the AS pin of the CH7023 (49-pin BGA package) is pulled low, the Device Address Byte becomes ECh for serial port write and EDh for serial port read. When the AS pin of the CH7023 (49-pin BGA package) is pulled high, the Device Address Byte becomes EAh for serial port write and EBh for serial port reads. The CH7023 (48-pin LQFP package) on the other hand does not have an external AS pin. The AS bit is internally tied to low.

After the DAB is received, the Chronitel encoder expects a Register Address Byte (RAB) from the master. The

data format of the RAB is shown below.

Device Address Byte (DAB)

CH7023 (49-pin BGA package) DAB

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	AS*	AS	R/W*

CH7023 (48-pin LQFP package) DAB

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	1	0	R/W*

AS Address Select

For the CH7023 (49-pin BGA package), the value of this bit is determined by the status of the AS pin. When the pin is strapped low, the value of AS = 0. When the pin is strapped high, the value of AS = 1. The CH7023 (48-pin LQFP package) does not have the AS pin.

R/W Read/Write Indicator

- “0”: The master device will write to the encoder at the register location specified by the address AR[7:0]
- “1”: The master device will read from the encoder at the register location specified by the address AR[7:0].

Register Address Byte (RAB)

B7	B6	B5	B4	B3	B2	B1	B0
AR[7]	AR[6]	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

AR[7:0] is the register address byte that specifies the address of the register to be accessed. The value of AR[7:0] will be loaded into the Address Register of the Chrontel encoder. The R/W access, which follows, will be directed to the register specified by Address Register.

2.3 Chrontel Encoder Write Cycle Protocol (R/W* = 0)

An acknowledge is required for all data transfers. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SPD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SPD line, during the acknowledge clock pulse, so that it remains LOW during the HIGH period of the clock pulse. Note that the resultant state of SPD is the wired-AND of data outputs from the transmitter and receiver. **Figure 2** shows the acknowledge protocol.

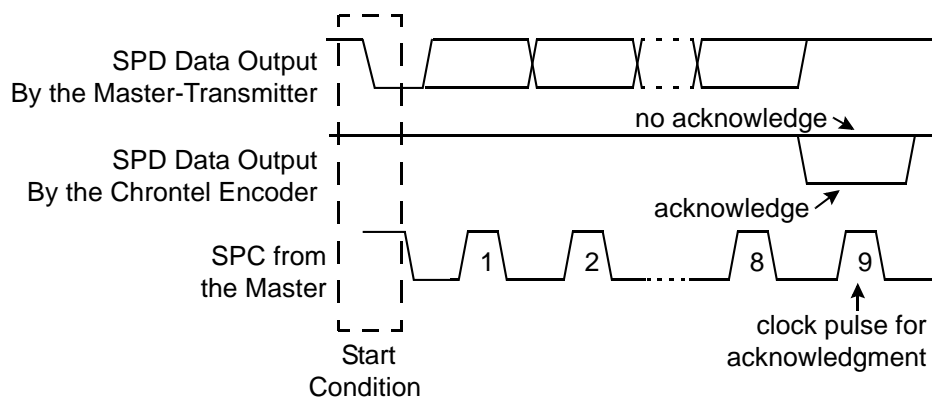
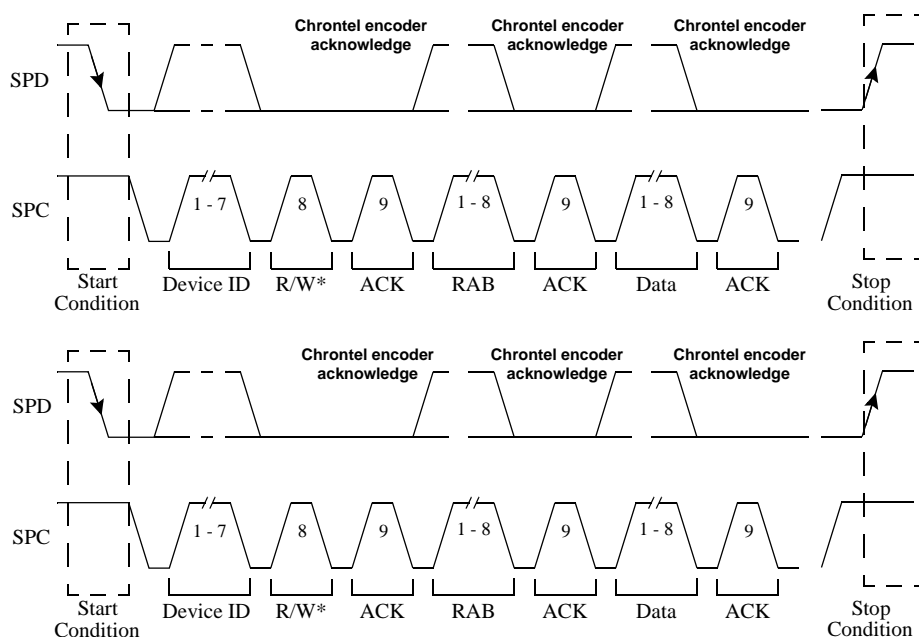


Figure 2: Acknowledge Protocol

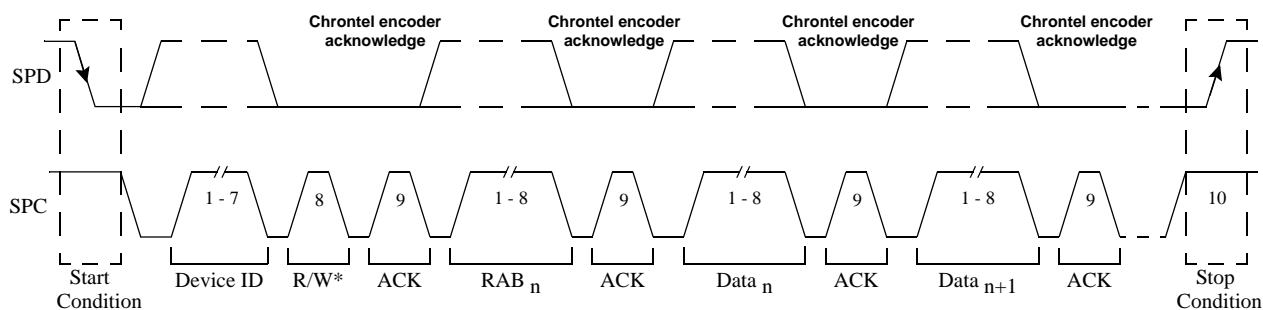
Figure 3 represents two consecutive Single step write cycles. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[7:0]. The serial interface bus will then enter the "Stop Condition" immediately after the acknowledge has been received. The cycle is then repeated for each subsequent write cycle.



Note: The acknowledge is from the Chrontel encoder (slave).

Figure 3: Single-step Write Cycles (2 cycles)

An Auto-increment write cycle is shown in **Figure 4**. During the Auto-increment write, the register address pointer continues to increment for each data write cycle until AR[7:0] = the last accessible Address Register of the encoder. The next byte of information represents a new auto-sequencing “Starting address”, which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new “Starting address”. The Auto-increment sequence can be terminated any time by either a “STOP” or “RESTART” condition. The write operation can be terminated with a “STOP” condition.



Note: The acknowledge is from the Chrontel encoder (slave).

Figure 4: Auto-Increment Write Cycle

2.4 Chrontel Encoder Read Cycle Protocol (R/W* = 1)

The master-receiver must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter encoder will then release the data line to allow the master to generate either the STOP condition or the RESTART condition.

To read the content of the registers, the master device must first issue a “START” condition (or a “RESTART”

condition). After the START condition, the first byte of data will be the DAB with R/W = 0. The second byte is the RAB with AR[7:0] containing the address of the register that the master device intends to read from. The master device must then issue a “RESTART” condition (“RESTART” = “START”, without a previous “STOP” condition). The first byte of data, after the RESTART condition, is another DAB with R/W=1, indicating the master’s intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). For Single-step read, a “Stop” condition or “Restart” condition is sent out immediately after the acknowledge which indicates that the data has been read (see **Figure 5**).

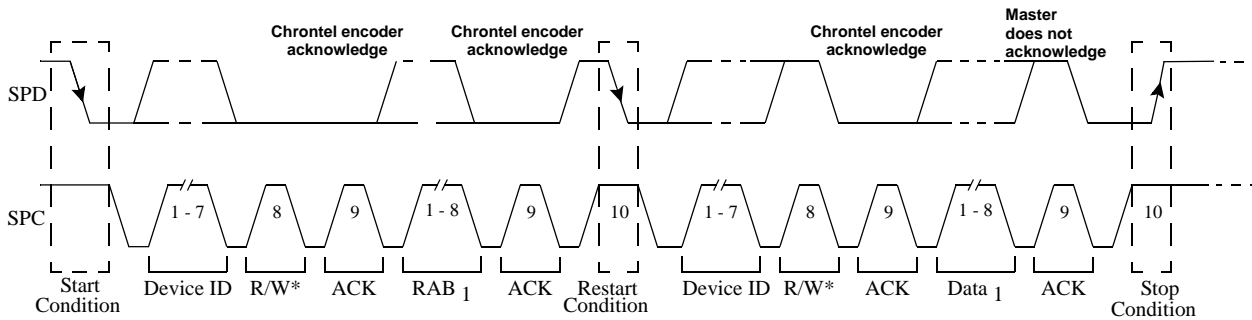


Figure 5: Single-step Read Cycles (2 cycles)

For Auto-increment read cycles, the address register is incremented automatically. This allows subsequent data bytes to be read from successive registers without having to provide a second RAB.

Regarding the Auto-increment read cycle, the address register continues to increment for each read cycle. When AR[7:0] of the RAB has been incremented to the last accessible register address of the encoder, the Address Register will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 6** shows an Auto-increment read cycle terminated by a STOP condition.

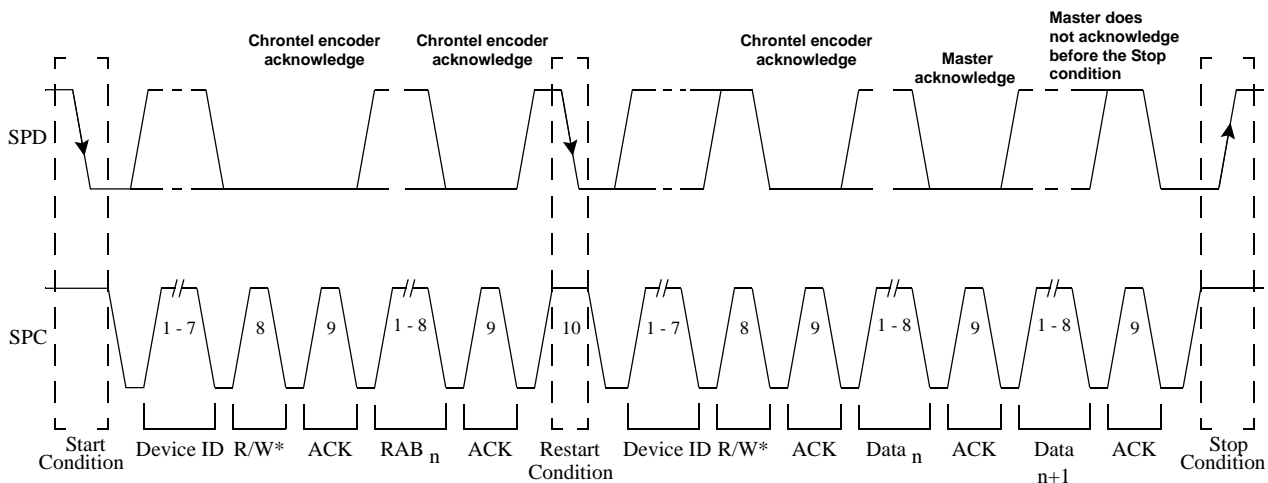


Figure 6: Auto-increment Read Cycles

3. Electrical Specifications

Table 1: DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	$I_{OL} = 2.0 \text{ mA}$			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		$V_{DDIO} + 0.5$	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V

Table 2: AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{SPC}	SPC clock frequency		0		400	kHz
$t_{LOW-SPC}$	Low Period of SPC clock		1.3			μs
$t_{HIGH-SPC}$	High Period of SPC clock		0.6			μs
t_{SU-SPD}	Data setup time		100			ns
t_{HD-SPD}	Data hold time		0			ns
t_{F-SPD}	Fall time of SPD signal	$C_{load} = 400\text{pf}$			300	ns

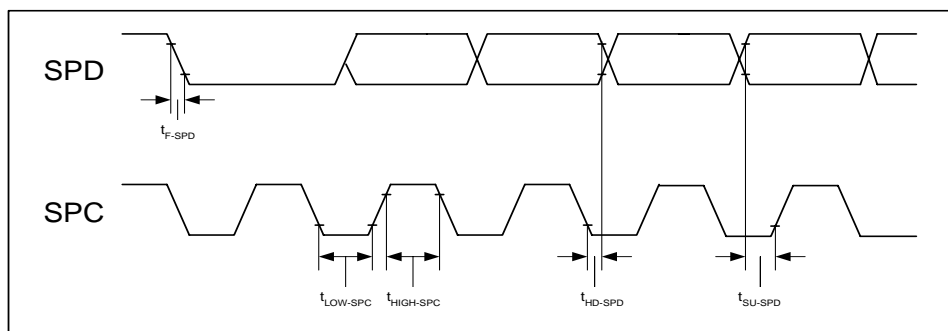


Figure 7: Serial Port Interface Timing

Appendix: Registers Maps of the CH7023 Encoder

Table 3: Non-Macrovision registers map of the CH7023

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
01h	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
02h								
03h							RESETIB	RESETDB
04h					PDDAC[1]	PDDAC[0]		FPD
05h		HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
06h		SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
07h		CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
08h	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
09h						TE[2]	TE[1]	TE[0]
0Ah	TV_BP	SVD/DDAC	DACSW[1]	DACSW[0]	VOS[3]	VOS[2]	VOS[1]	VOS[0]
0Bh	XTALSEL				XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]
0Ch	DUCVBS	DCKSEL						MULTI
0Dh	HIGH	REVERSE	SWAP[2]	SWAP[1]	SWAP[0]	IDF[2]	IDF[1]	IDF[0]
0Eh	POUTEN	DES	FLDSEN	FLDS	HPO	VPO	SYO	DIFFEN
0Fh	XCH	CFRB	CFBP	CBW	YSV[1]	YSV[0]	YCV[1]	YCV[0]
10h						AFF[2]	AFF[1]	AFF[0]
11h	HVAUTO		HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
12h	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
13h	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
14h				HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
15h	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
16h	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
17h			VO[9]	VO[8]	VTI[9]	VTI[8]	VAI[9]	VAI[8]
18h	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
19h	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
1Ah	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
1Bh			VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
1Ch				ACIV	BSTADJ[2]	BSTADJ[1]	BSTADJ[0]	DOTCRB
1Dh				DACCKINV	DKINV	PKINV	CKINV	UKINV
1Eh						TVHA[10]	TVHA[9]	TVHA[8]
1Fh	TVHA[7]	TVHA[6]	TVHA[5]	TVHA[4]	TVHA[3]	TVHA[2]	TVHA[1]	TVHA[0]
20h							VP[1]	VP[0]
21h	VP[9]	VP[8]	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]
22h							HP[1]	HP[0]
23h	HP[9]	HP[8]	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]
24h	A[31]	A[30]	A[29]	A[28]	A[27]	A[26]	A[25]	A[24]
25h	A[23]	A[22]	A[21]	A[20]	A[19]	A[18]	A[17]	A[16]
26h	A[15]	A[14]	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]
27h	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
28h	P[23]	P[22]	P[21]	P[20]	P[19]	P[18]	P[17]	P[16]
29h	P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]
2Ah	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]
2Bh	N[23]	N[22]	N[21]	N[20]	N[19]	N[18]	N[17]	N[16]
2Ch	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
2Dh	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
2Eh	T[7]	T[6]	T[5]	T[4]	T[3]	T[2]	T[1]	T[0]
2Fh			PLL2N2[2]	PLL2N2[1]	PLL2N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
30h			PLL3N4[2]	PLL3N4[1]	PLL3N4[0]	PLL3N3[2]	PLL3N3[1]	PLL3N3[0]
31h						PLL3N5[2]	PLL3N5[1]	PLL3N5[0]
32h	FSCISPP[15]	FSCISPP[14]	FSCISPP[13]	FSCISPP[12]	FSCISPP[11]	FSCISPP[10]	FSCISPP[9]	FSCISPP[8]
33h	FSCISPP[7]	FSCISPP[6]	FSCISPP[5]	FSCISPP[4]	FSCISPP[3]	FSCISPP[2]	FSCISPP[1]	FSCISPP[0]
34h						SCFREQ[26]	SCFREQ[25]	SCFREQ[24]
35h	SCFREQ[23]	SCFREQ[22]	SCFREQ[21]	SCFREQ[20]	SCFREQ[19]	SCFREQ[18]	SCFREQ[17]	SCFREQ[16]
36h	SCFREQ[15]	SCFREQ[14]	SCFREQ[13]	SCFREQ[12]	SCFREQ[11]	SCFREQ[10]	SCFREQ[9]	SCFREQ[8]
37h	SCFREQ[7]	SCFREQ[6]	SCFREQ[5]	SCFREQ[4]	SCFREQ[3]	SCFREQ[2]	SCFREQ[1]	SCFREQ[0]
38h								
39h								
3Ah								
3Bh								
3Ch								
3Dh								
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58h								
59h								
5Ah								
5Bh								
5Ch								
5Dh								
5Eh								
5Fh								
60h								
61h								
62h	SENSEEN							
63h							SEL_R	
64h								
65h								
66h								
67h								
68h								
69h								
6Ah								
6Bh								
6Ch								
6Dh								
6Eh								
6Fh								
70h								
71h								
72h								
73h								
74h								
75h								
76h								
77h								
78h								
79h								
7Ah								
7Bh								
7Ch								
7Dh								
7Eh			AT TACH2[1]	AT TACH2[0]	AT TACH1[1]	AT TACH1[0]	AT TACH0[1]	AT TACH0[0]
7Fh								

4. Revision History

Rev. #	Date	Section	Description
1.0	2/15/06	All	First official release.

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