



## A list of different for the CH7004C, CH7005C and CH7007A

	CH7007A	CH7005C	CH7004C
<b>Package Foot Print</b>	Not compatible with CH7005C	Not compatible with CH7007A	Same as CH7005C except ADDR pin.
<b>Function of Pin 35 PLCC or Pin 29 TQFP</b>	RESET*(Reset input)	RESET*(Reset input)	ADDR (Address select)
<b>D/A Converter Reference Resistor Pin Symbol (Pin 30 PLCC or Pin 24 TQFP).</b>	ISET	RSET	RSET
<b>DS/BCO Pin 41 PLCC or Pin 35 TQFP. (Please contact application engineer for detail).</b>	In some application , it is recommended to use SAV register 07H instead of using DS as input to start the active pixel.	Same as CH7007A	Output as buffered clock only.
<b>Power ON Default Setting (Please refer the data sheet for more detail of the register's default value).</b>	The device is in full power down mode except I <sup>2</sup> C circuit. When it is out of power down mode, P-OUT pin will be tri-stated, device is in slave mode and DS/BCO pin will be configured as input.	The device is in normal ON mode. The P-OUT pin will be in tri-stated, device is in slave mode and DS/BCO pin will be configured as input.	The device is in normal ON mode. BCO pin is an output only configuration and the device is in slave mode.
<b>Power Supply Requirement</b>	5V, 3.3V and scaleable I/O voltage from 1.8V to 3.3V.	5V and 3.3V	5V and 3.3V (for internal digital circuit used only).
<b>Scaleable I/O Voltage</b>	DS/BCO input pin, HSYNC and VSYNC input pin, Data bus and P-OUT output pin.	N/A	N/A
<b>XO and XI pins for external CMOS clock connection.</b>	As specified, XI/FIN pin for external clock connection and XO pin not connected.	XI pin is grounded and XO/FIN pin for external clock connection. In order to have same configuration as CH7007A, please contact application engineer for detail.	Same as CH7005C.

# CHRONTEL

	CH7007A	CH7005C	CH7004C
<b>SD and SC (I<sup>2</sup>C interface port).</b>	3.3V compatible.	3.3V compatible.	5V compatible (Please refer TB13 for 3.3V interface).
<b>Data Bus Width</b>	8 or 12 bit	8, 12 or 16 bits	Same as CH7005C
<b>GPIO Ports</b>	2	N/A	N/A
<b>XCLK</b>	Differential XCLK is available	N/A	N/A
<b>I/O Reference Pin</b>	VREF pin.	N/A	N/A
<b>Operation Mode</b>	Master and Slave mode	Master and Slave mode	Same as CH7005C except no master syncs
<b>Pass Through Mode</b>	N/A	Yes	Yes
<b>CCIR Compatibility</b>	CCIR656	CCIR601/656	Same as CH7005C
<b>Multiplexed / Non-Multiplexed Mode (Please refer data sheet for detail).</b>	8 or 12 bits multiplexed with 2X pixel data rate	8, 12 and 16 bits multiplexed with 2X or 3X pixel data rate. 15 or 16 bits non-multiplexed	Same as CH7005C
<b>Number of Display Mode</b>	27	29	29
<b>Device ID</b>	50H	3AH	32H
<b>Macrovision Support</b>	Yes	Yes	Yes
<b>Address Registers Map</b>	Address registers are the same as CH7005C. There are few extra feature bits available in CH7007A. Please refer the data sheet for detail.	Please refer the data sheet for detail.	Same as CH7005C except registers 1BH bit 4 (P-OUTP) and 1CH bit 4 (DSEN). Please refer CH7004C's data sheet for detail.