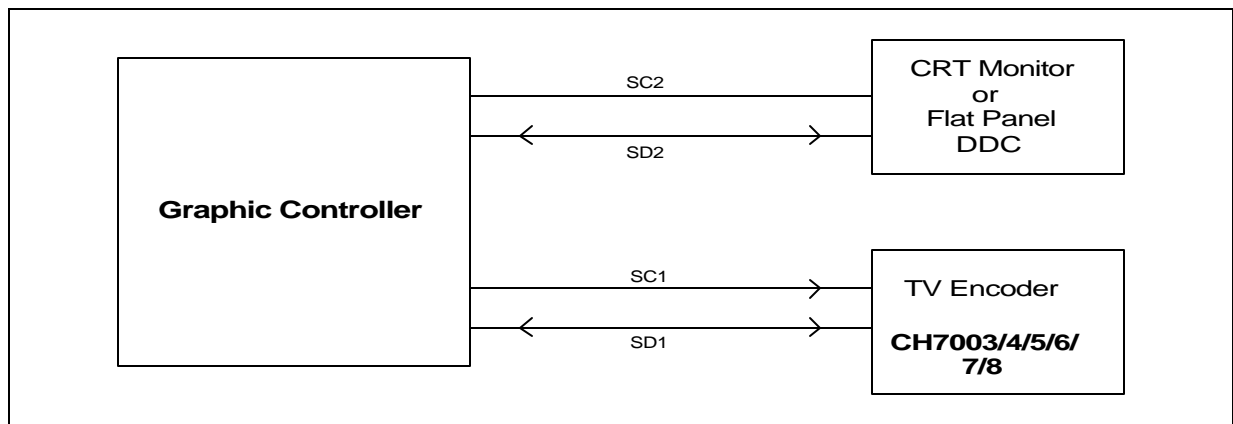


IIC tranreceiver with CH7003/4/5/6/7/8 under multiple display environment

Chrontel TV encoder has the capability to access the internal register through IIC interface. This interface is configured and activated by the graphic controller through the use of serial clock. The graphic controller or equivalent device is using serial clock to synchronous the serial data such that the serial data can be read from or written to the TV encoder.

Within the PC system, the display devices (Flat panel and CRT monitor) are multiplex the IIC lines with other function; i.e. audio chip, MPEG decoders... etc; and the display devices have potential to hold the serial clock line in low voltage level. Because of the IIC bus sharing among different devices within the PC system, corruption of IIC under multiple display may happen. Carefully handle the physical connection of IIC lines and register address byte in the software routine will reduce the corruption of IIC bus signalling.

We have not exhausted ourselves to investigate all the possible usage of IIC bus within the PC system, any feedback from the PC manufacturers are welcome to improve the application of IIC bus. **The ideal solution is not to use the same IIC lines to connect IIC display devices inside the PC and DDC devices outside the PC.** Please refer to the diagram below:



Note: Please consults application engineer if customers want to use the same IIC bus for TV encoder & CRT monitor or Flat Panel DDC with strip optional configuration.

Regardless the use of separate IIC line or the design is done using the same IIC bus for the display DDC. It is recommended to set the RAB (Register Address Byte); the bit 7 to 1 (Please refer CH7007/4/5/6/7/8 data sheet; IIC port operation) in the software routine. This bit setting is applied to both the Alternating and Auto-Increment mode.

Other concern is that, if mixed voltage (3.3V IIC bus and 5V IIC bus) design is required within the system, please consult application engineer for the detail.