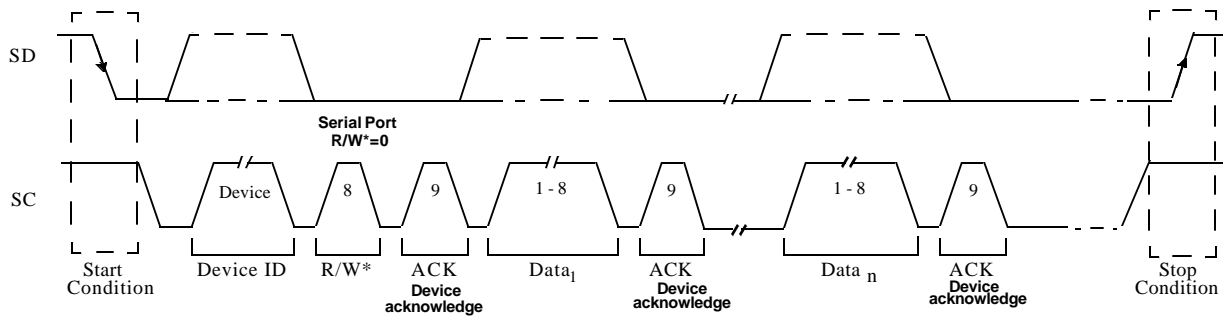


## Serial Port Operation for CH7002-CH7008, CH5001, CH5101 and CH5002

- \* CH700x will be used to represent CH7002 - CH7008.
- \* CH5x0x will be used to represent CH5001, CH5101 and CH5002.

### Transfer Protocol

Both read and write operation can be executed in “Alternating” and “Auto-increment” modes. Alternating mode expects a register address prior to each read or write from that location (i.e., transfers alternate between address and data). Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data...). A basic serial port transfer protocol is shown in **Figure 1** and described below.



**Figure 1: Serial Port Transfer Protocol**

1. The transfer sequence is initiated when a high-to-low transition of SD occurs while SC is high; this is the “START” condition. Transitions of address and data bits can only occur while SC is low.
2. The transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high; this is the “STOP” condition.
3. Upon receiving the first START condition, the CH700x/CH5x0x expects a Device Address Byte (DAB) from the master device. The value of the device address is shown in the DAB data format below.
4. After the DAB is received, the CH700x/CH5x0x expects a Register Address Byte (RAB) from the master. The format of the RAB is shown in the RAB data format below (note that B7 is not used).

### Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	0	1	R/W

### R/W

### Read/Write Indicator

- “0”: master device will write to the CH700x/CH5x0x at the register location specified by the address AR[5:0]
- “1”: master device will read from the CH700x/CH5x0x at the register location specified by the address AR[5:0].

**Register Address Byte (RAB)(Please refer to the data sheet for detail)**

B7	B6	B5	B4	B3	B2	B1	B0
1	AutoInc	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

**AutoInc Register Address Auto-Increment - to facilitate sequential R/W of registers.**

“1”: Auto-Increment enabled (auto-increment mode).

Write: After writing data into a register, the Address Register will automatically be incremented by one.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will automatically be incremented by one. However, for the first read after an RAB, the Address Register will not be changed.

“0”: Auto-Increment disabled (alternating mode).

Write: After writing data into a register, the Address Register will remain unchanged until a new RAB is written.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will remain unchanged.

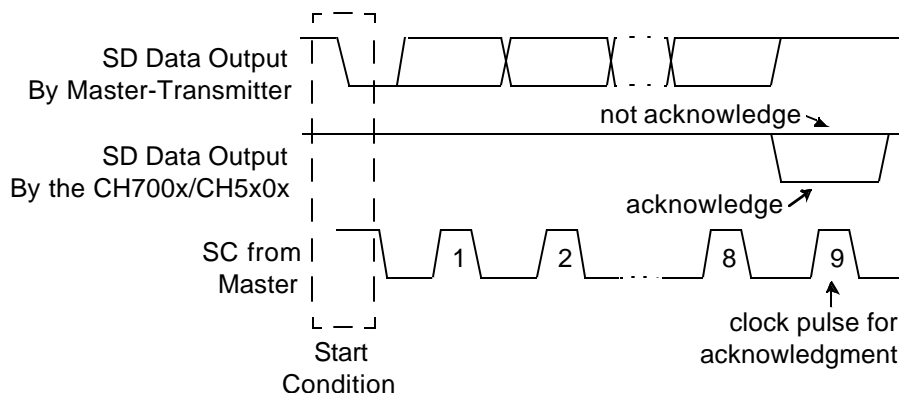
**AR[5:0] Specifies the Address of the Register to be Accessed.**

This register address is loaded into the Address Register of the CH700x/CH5x0x. The R/W access, which follows, is directed to the register specified by the content stored in the Address Register.

The following two sections describe the operation of the serial interface for the four combinations of R/W = 0,1 and AutoInc = 0,1.

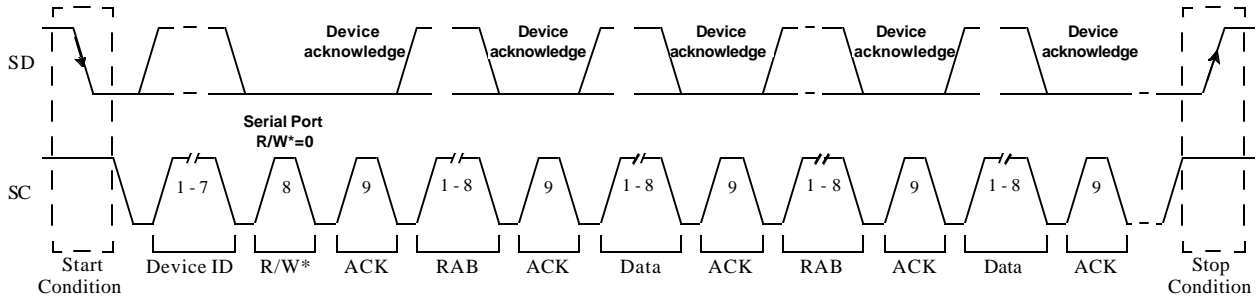
**CH700x/CH5x0x Write Cycle Protocols (R/W = 0)**

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH700x/CH5x0x always acknowledges for writes (see **Figure 2**). Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver.



**Figure 2: Acknowledge on the Bus**

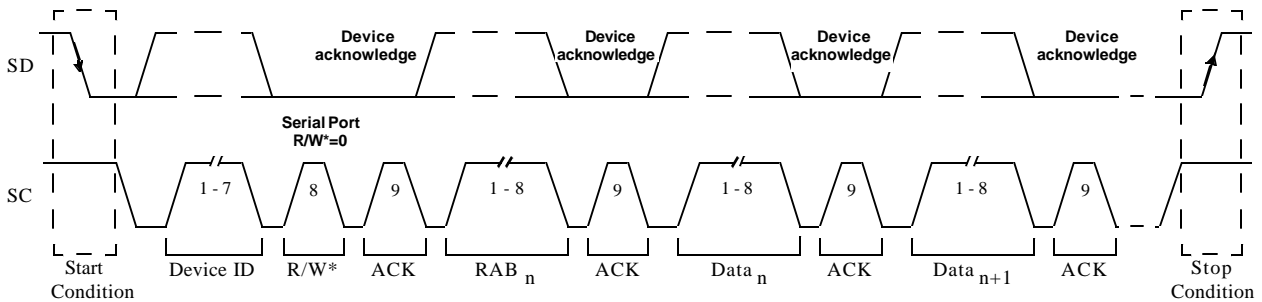
**Figure 3** shows two consecutive alternating write cycles for AutoInc = 0 and R/W = 0. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[5:0]. If AutoInc = 0, then another RAB is expected from the master device, followed by another data byte, and so on.



**Note:** The acknowledge is from the CH700x/CH5x0x (slave).

**Figure 3: Alternating Write Cycles**

If AutoInc = 1, then the register address pointer will be incremented automatically and subsequent data bytes will be written into successive registers without providing an RAB between each data byte. An Auto-increment write cycle is shown in **Figure 4**.



**Note:** The acknowledge is from the CH700x/CH5x0x (slave).

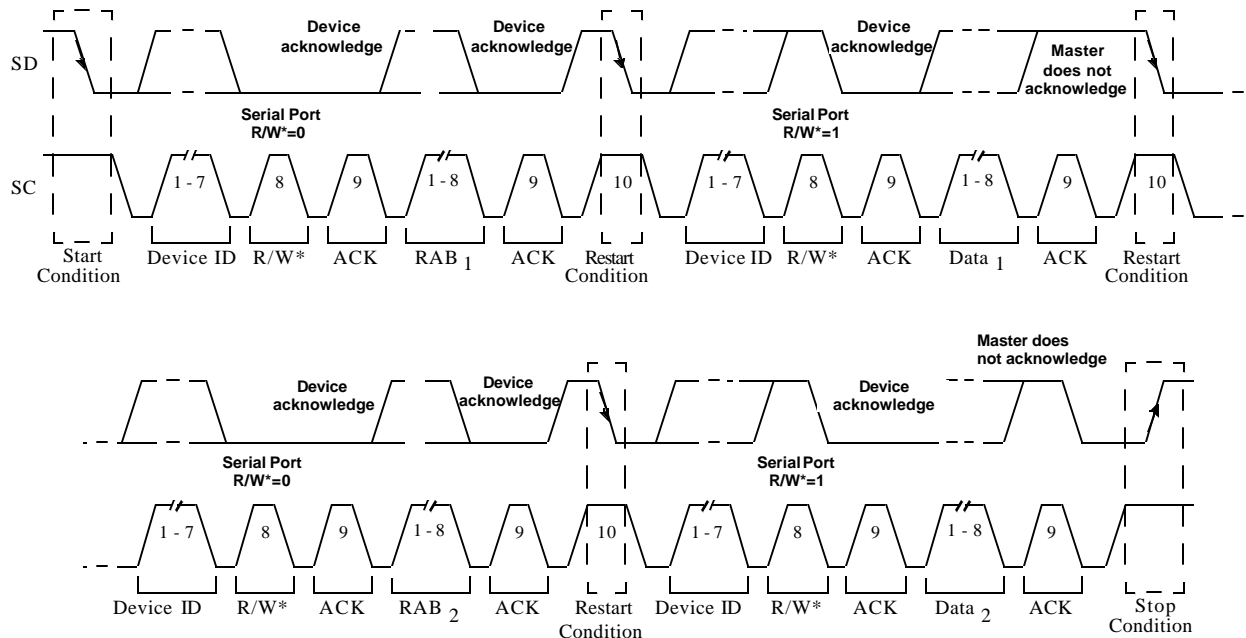
**Figure 4: Auto-Increment Write Cycle**

When the auto-increment mode is enabled (AutoInc is set to 1), the register address pointer continues to increment for each write cycle until AR[5:0] = 3F (3F is the address of the Address Register). The next byte of information represents a new auto-sequencing “Starting address”, which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new “Starting address”. The auto-increment sequence can be terminated any time by either a “STOP” or “RESTART” condition. The write operation can be terminated with a “STOP” condition.

**CH700x/CH5x0x Read Cycle Protocols (R/W = 1)**

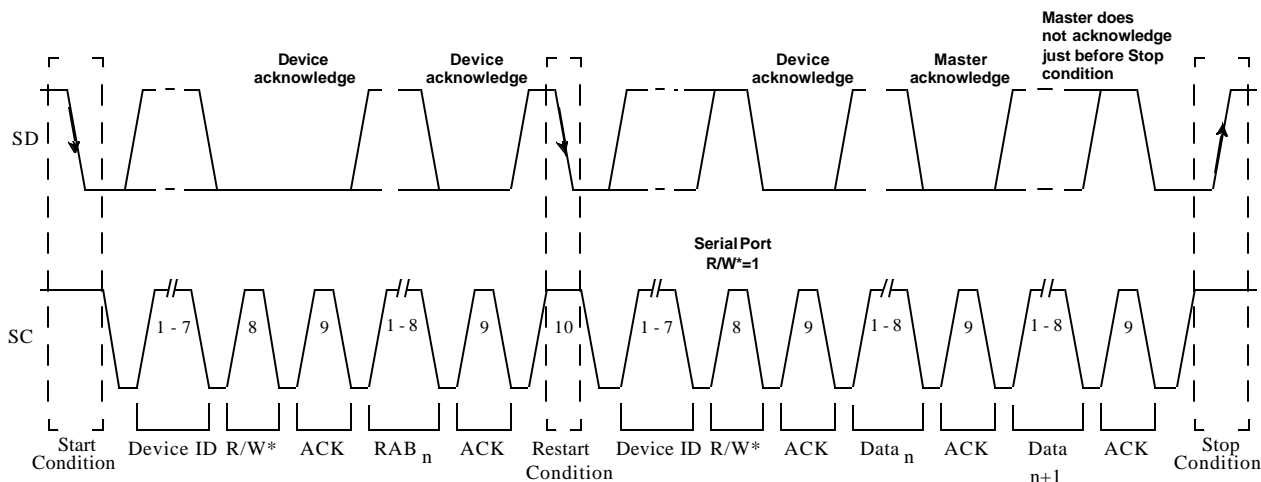
If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH700x/CH5x0x releases the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device starts by issuing a “START” condition (or a “RESTART” condition). The first byte of data, after the START condition, is a DAB with R/W = 0. The second byte is the RAB with AR[5:0], containing the address of the register that the master device intends to read from in AR[5:0]. The master device should then issue a “RESTART” condition (“RESTART” = “START”, without a previous “STOP” condition). The first byte of data, after this RESTART condition, is another DAB with R/W=1, indicating the master’s intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). If AutoInc = 0, then another RESTART condition, followed by another DAB with R/W = 0 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. After that, the master may read another data byte, and so on. In summary, a RESTART condition, followed by a DAB, must be produced by the master before each of the RAB, and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 5**.



**Figure 5: Alternating Read Cycle**

If AutoInc = 1, then the address register will be incremented automatically and subsequent data bytes can be read from successive registers, without providing a second RAB.



**Figure 6: Auto-increment Read Cycle**

When the auto-increment mode is enabled (AutoInc is set to 1), the Address Register will continue incrementing for each read cycle. When the content of the Address Register reaches 2A, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 6** shows an auto-increment read cycle terminated by a STOP or RESTART condition.