

PC Motherboard with CH7009 Design Consideration

The Placement for CH7009 on the PC Motherboard

It is suggested that CH7009 be placed close to graphics controller chipset to reduce the length of interconnecting traces. The Ch7009 should be positioned between the graphics controller and the edge of the board that houses the DVI connector. It should position directly behind the DVI connector. Figure 1 shows a reference placement for CH7009 on a PC motherboard. The COM1 connector on the back edge of the motherboard should be removed and replaced with a DVI connector. A back panel bracket will contain a COM1, an RCA composite, and an S-video mini DIN connectors. An S-video and RCA composite video interface header (4 x 2 pins) and a COM1 interface header (5 x 2 pins) should be added on the motherboard as shown in Figure 1. Figure 2 shows the back panel bracket configuration with a ribbon cable and a 75 ohm shielded cable connecting to the corresponding interface headers (COM1 and S-video, composite video, respectively) on the motherboard. It is recommended that the CH7009 be placed as close as possible to the DVI connector. In general, if the differential impedance (100 ohm for DVI signaling) or the characteristic impedance (75 ohm for TV-out signaling) can be maintained, the length of the trace has no limit. Maintaining these impedance is, however, impractical for long distances on a motherboard. As there are either high speed (up to 1.7 Gbs) or analog (TV-out) signals, it is important to minimize these points of signal degradation. To avoid impedance mismatch from the traces which will cause signal degradation, short and straight traces should be considered to minimize the vias, bends and no 90 degree corners. These signals must be routed exclusively above a solid power plane (no breaks in power plane). These signals must also be shielded from other signals which might interfere or be interfered with. This is accomplished with a combination of physical separation and shielding with power plane traces. Shielding is costly from a standpoint of motherboard real estate, however, it is a must.

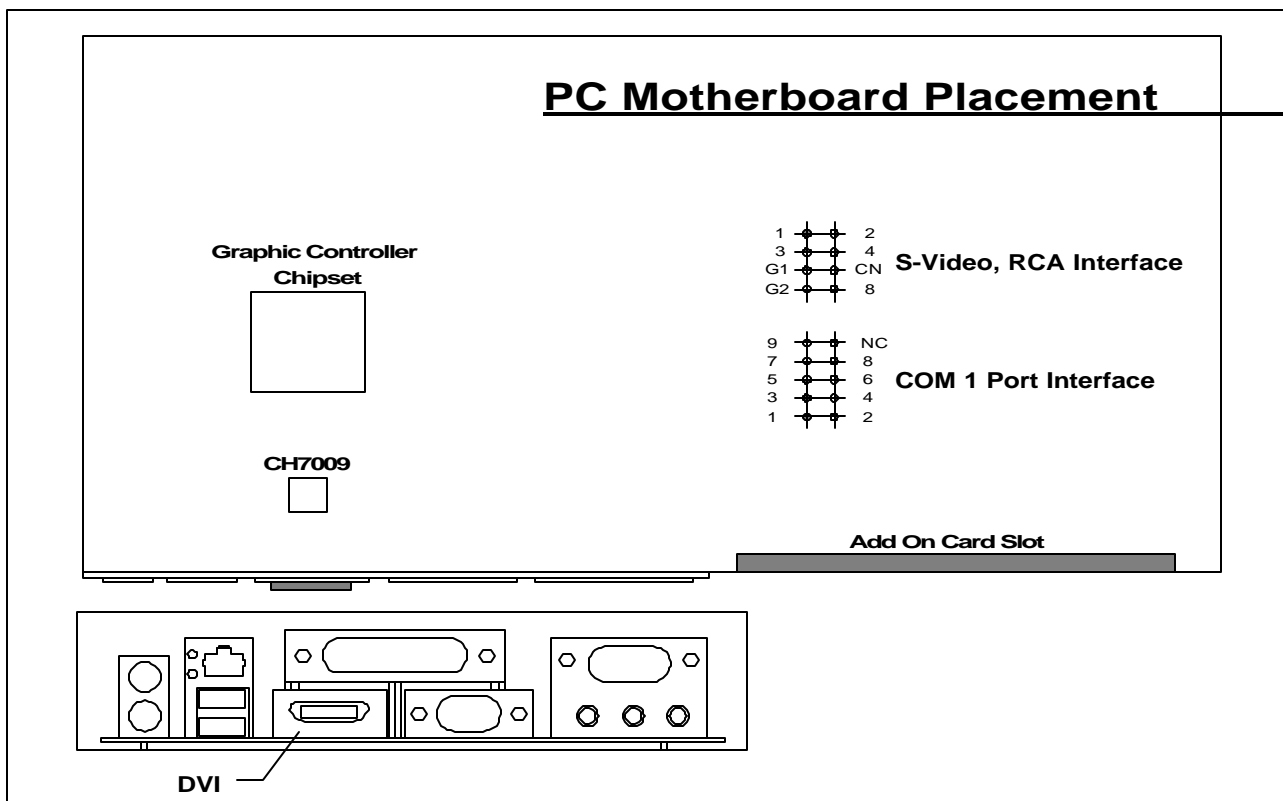


Figure 1. Reference Placement for CH7009 on a PC Motherboard

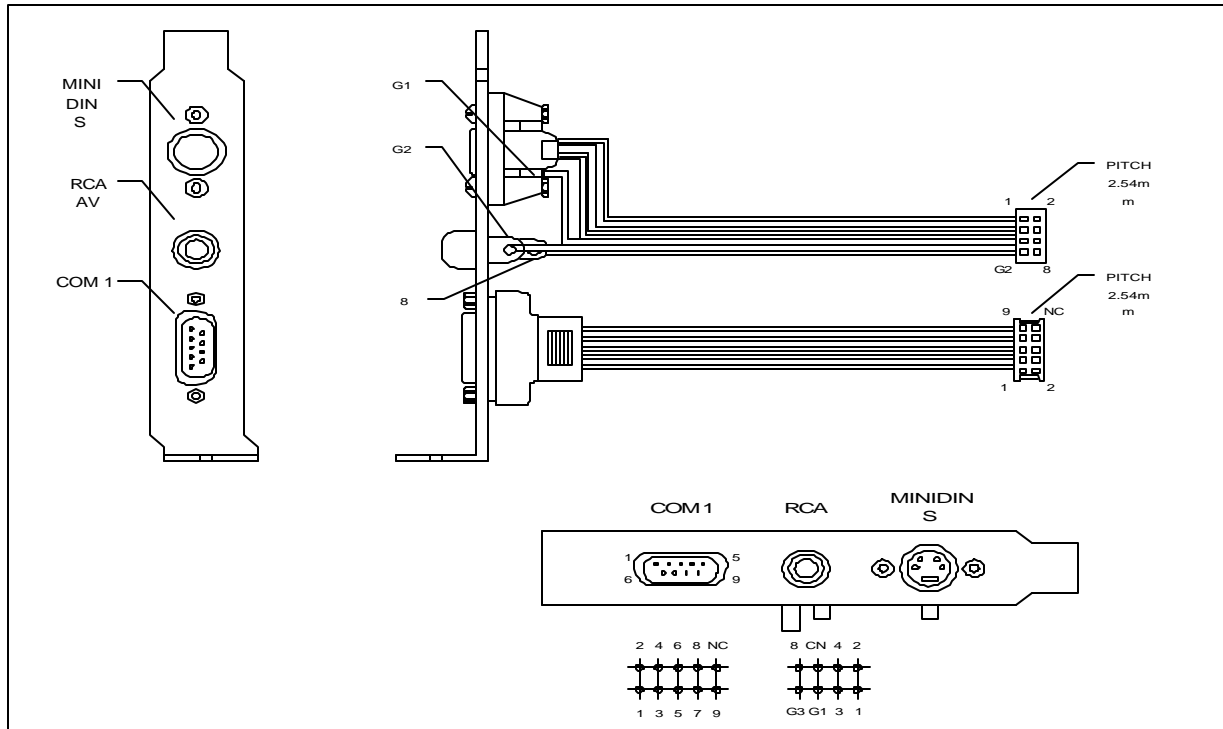


Figure 2. Reference Back Panel Bracket Configuration for CH7009 TV Out

Both board real estate and signal degradation are minimized by keeping the CH7009 in close proximity to the physical connectors. Also, chip orientation requires attention as it can have an effect on the ultimate trace length as well.

The Layout Consideration for CH7009 Signals

Two sets of critical busses and TV output signals need to be managed carefully. They are described as follows:

- (1) 4 pairs of high speed (> 1GHz) differential pair output signals (RGB & Clock) between CH7009 and DVI connector:
 - Keep traces short, straight (minimize vias and bends and no 90 degree corners).
 - Each differential pair must remain matched (trace should be routed together).
 - Route trace as 50 ohm transmission line.
- (2) Graphics controller and CH7009 interface signals:
 - 17 pin signals from graphics controller with critical setup / hold time: (12 bit data, 2 syncs, 2 clocks, Data enable)
 - Keep these traces matched.
 - Decoupling capacitors should be placed as close to CH7009 as possible, and should be connected directly to device pins.
- (3) TV Output Signal Requirement:
 - Shield luma channel of S-Video output to prevent coupling from chroma or CVBS output.
 - Make adequate spacing between inductors in output reconstruction filters.
 - Use 75 ohm termination resistors placed close to CH7009 and use pin 34 ground.
 - On chip crystal oscillator is required for TV output function.

For more details of PCB layout and design consideration, please refer to Application note AN-34.