



Upgrading From CH7003B to CH7013A for TV-Out Application

Guideline to Hardware Modification

Technically speaking, CH7013A is function and pin to pin compatible to CH7003B. However, CH7013A provides text enhancement capability which CH7003B doesn't, and it has more selections for flicker filtering than CH7003B does. Nothing needs to be changed in the hardware design. However, if the SCART type I output is considered, the connection from CSYNC at Pin 17 of CH7013A needs a slight modification. Please see Application Note AN-38 for details.

Guideline to Software Modification

In order to make the migration of application design from using CH7003B to CH7013A smoothly, the following guideline for the software modification should be followed carefully:

- Version ID** Register VID
Address 25H

CH7003B = 02H
CH7013A = 32H

- Control Bits**

The following control register bits need to be modified in order to use CH7013A properly:

Address 10H bit[7:4] = 0 and bit[3:0] = same setting as CH7003B
Address 3DH bit[2:0] = 0 and bit[7:3] = don't care

- Address Register** Register AR
Address 3FH

CH7003B = N/A
CH7013A = don't care

- Flicker Filtering** Register FFR
Address 01H

I) CH7003B

FFR[1:0] Scaled Modes (non 1/1 scale ratio)			FFR[1:0] Non-scaled Modes (1/1 ratio)		
FF1	FF0		FF1	FF0	
0	X	3 line flicker filter, moderate flicker reduction.	0	0	Disable flicker filtering.
			0	1	Moderate flicker filtering (default mode).
1	X	4 line flicker filter, minimum flicker reduction.	1	0	Low flicker reduction.
			1	1	High flicker reduction.

II) CH7013A

FFR[5:2]				Control Functions	
FC1	FC0	FY1	FY0	Channel	Descriptions
		0	0	Luma	Minimal flicker filtering (default mode)
		0	1		Slight flicker filtering
		1	0		Maximum flicker filtering
		1	1		Invalid
0	0			Chroma	Minimal flicker filtering (default mode)
0	1				Slight flicker filtering
1	0				Maximum flicker filtering
1	1				Enable chroma dot crawl reduction

5. Text Enhancement Register FFR Address 01H

The Text Enhancement function is not available in CH7003B.

In CH7013A, the register setting for Text Enhancement is shown as the table below.

- CH7013A

FFR[1:0]		Control Functions
FT1	FT0	Descriptions
0	0	Maximum text enhancement
0	1	Slight text enhancement
1	0	Minimal text enhancement
1	1	Invalid

Note: When writing to Register 01H of CH7013A, FY[1:0] is bits 3:2 and FT[1:0] is bits 1:0. When reading from the Register 01H, FY[1:0] is bits 1:0 and FT[1:0] is bits 3:2.

6. Calculated Increment Value Register CIV

In CH7013A, Register CIV is using 26 bits value instead of 24 bits value as in CH7003B.

Register	Contents in CH7003B	Contents in CH7013A
21H[4:3]		CIV[25:24]
22H[7:0]	CIV[23:16]	CIV[23:16]
23H[7:0]	CIV[15:8]	CIV[15:8]
24H[7:0]	CIV[7:0]	CIV[7:0]