



A Guideline to Minimize Noise in TV Encoder Caused by Noisy DC Power Source

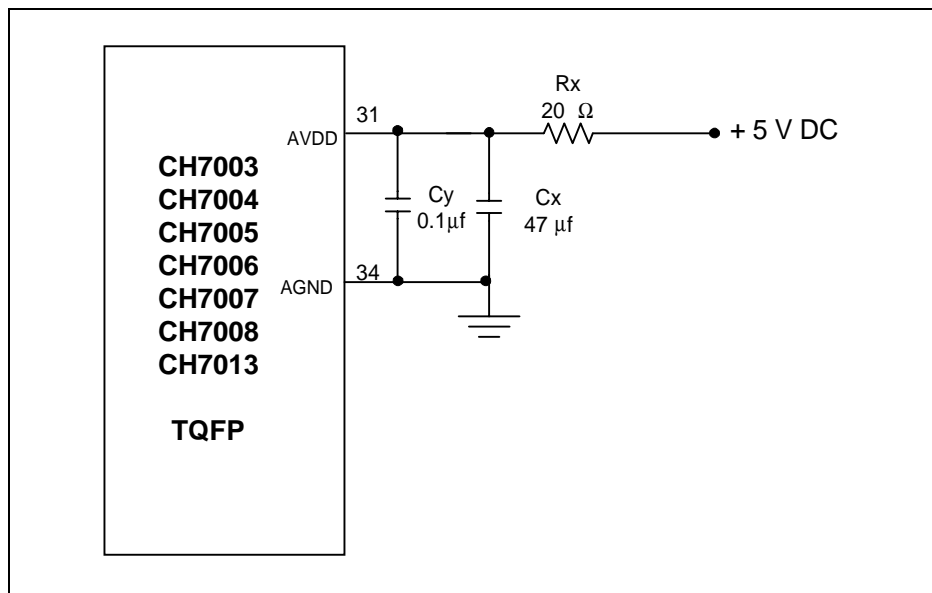
Description of Problem

A noisy DC power source to AVDD (power source for PLL) of CH70XX chip may generate visual noise in TV display.

Solution to the Problem

It is suggested that a low pass RC filter be constructed between +5V DC source and AVDD (power source for PLL) of CH70XX chip. The filter should be placed close to the AVDD pin, so that the distance between the output of the filter and the pin can be short. In addition, add a 0.1 μf cap between the pin AVDD and AGND to filter out the extra high frequency noise.

Schematics



Schematics of Low Pass Filter to Minimize the Noise Going to PLL Circuit

Details

Given $R_x = 20$ ohms and $C_x = 47 \mu\text{f}$, the corner frequency of the filter, $f_c = 1 / (2\pi R_x C_x) = 169$ Hz. It should filter out most of the low frequency and high frequency noise. The normal DC bias current from AVDD to the PLL circuit is 10 to 15 mA. Therefore, the voltage drop across the R_x is about 0.2 to 0.3 V, and this causes AVDD = 4.45 V to 4.95 V (with input VDC = 5 V +/- 5%) in the worst case. Under such working voltage, the PLL will be functioning normally by design.

C_y is added to filter out high frequency noise.