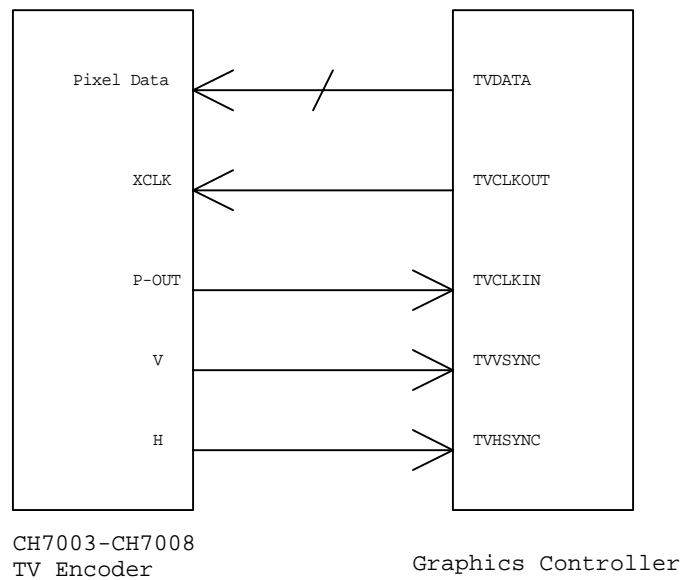


## A Special Treatment for H Sync in Sync-Master Mode

### Problem Description

In the application where the TV encoder operates in sync-master mode, the TV encoder generates its own H sync while giving out this signal and the pixel clock to the graphics controller (as shown in **Figure 1**). The pixel clock, used to generate data in the graphics controller, is fed back to the encoder. The new clock then works with the H sync and V sync to produce the encoded data for the TV set.



**Figure 1: The signal directions for the encoder-controller interface.**

The clocks generated in two different devices are not guaranteed to have the exactly same frequencies. Therefore, there exists a certain value of phase difference and it may fluctuate occasionally. When operating in sync-master mode, however, the TV encoder has to use its own sync signals, with this unsynchronized clock and the pixel data from the VGA controller, to generate TV-encoded signals. The situation is unpredictable when there is interference within or between these two devices.

The time lag for the original clock (P-OUT) and the returned clock (XCLK) can be variable and intermittently cause the H sync to lead a cycle, hence the data in each line may lose one bit in this line. The spontaneous change of the phase difference between H sync and XCLK may eventually shift one cycle to the next. As a result, the picture looks wavy.

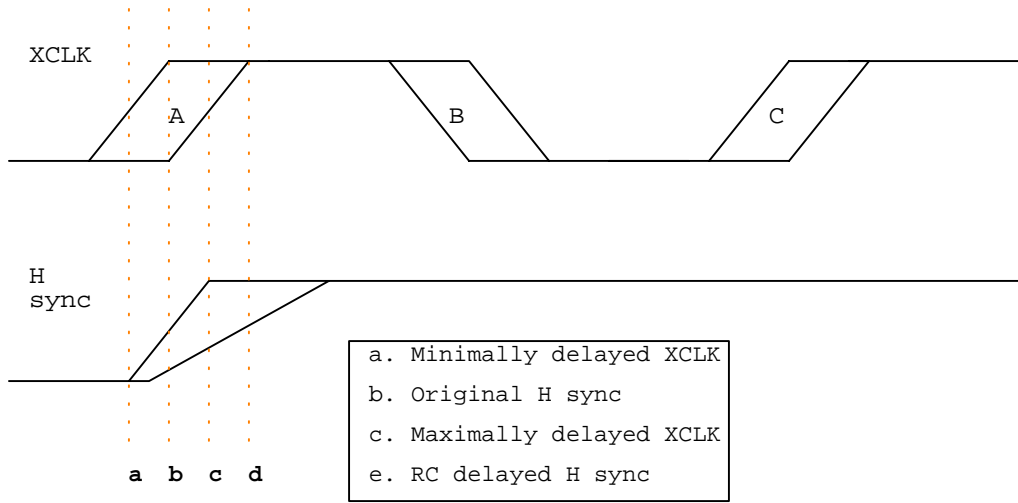
### Timing Analysis

The XCLK is the pixel clock generated by the graphics controller and does not always synchronize with P-OUT. Therefore, there may be a slight and variable phase change between them momentarily. Since H sync is originally clocked out by P-OUT, the phase change creates a problem for the data processing in the TV encoder due to the timing violation.

**Figure 2** shows the timing diagrams of XCLK and H sync with respect to each other. If we assume that H sync is fixed,

there are two situations can happen: 1) the H sync is ahead of XCLK or 2) the H sync is behind XCLK. Also assume that the H sync is clocked out at the positive edge of XCLK. For the non-multiplexed data mode, the sampling can be either in Area A or Area C. However, for the multiplexed data mode, the sampling is either in Area A or Area B.

In **Figure 2**, allowing line **b** to move beyond line **c** is to ensure the clocking not in Area A. Introducing a long delay, however, may push the clocking to happen in the stage even later than Area B for the multiplexed data mode, thus creating another problem. Therefore, we realize that in the high resolution display mode and using the multiplexed data mode for encoding, the problem is likely more severe.



**Figure 2: Timing analysis of XCLK and H sync.**

If we make an appropriate delay for H sync so that the clocking of H sync happens only in Area B for the multiplexed data mode and in Area C for the non-multiplexed data mode, the out-of-sync problem can be solved.

### Recommended Approaches

The unpredictable small change of phase difference between two signals is inherent in the electronic system in which no synchronization is present. The source of the H sync problem comes from the unsynchronization of P-OUT and XCLK, with H sync clocked out by P-OUT, not XCLK. However, the TV encoder generates TV-encoded data by H sync clocked by XCLK, not P-OUT. Therefore, as long as we lock the phase between P-OUT and XCLK, H sync will run as we wish. Since these two pins are in the TV encoder, we may use a phase-lock loop (PLL) to solve the problem.

If we tackle this problem by a by-pass route for P-OUT to reach XCLK, the synchronization is solved. However, the pixel data generated by the VGA controller will not be in tune with XCLK, consequently showing the data loss on the screen occasionally.

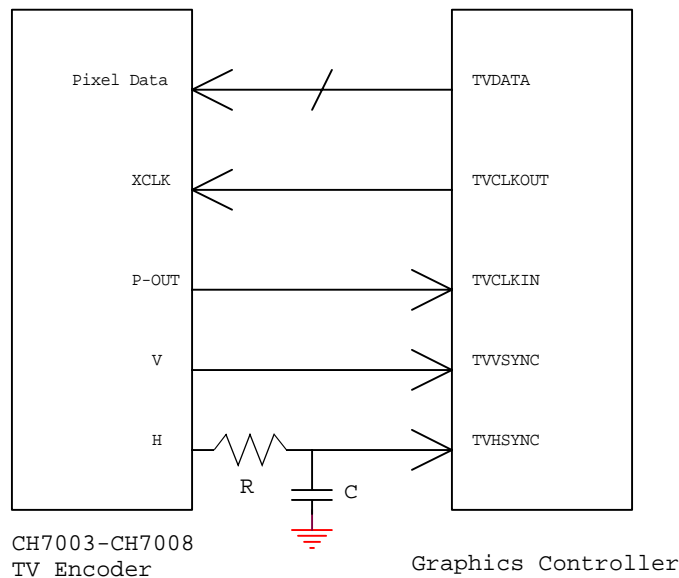
If a modification of the integrated circuit is not possible, we may delay the rise or fall time of H sync for XCLK to clock out in the next edge. This approach is feasible, because the amount of shift is small and a small capacitor is enough for this purpose. For higher frequencies the capacitance should be more carefully arranged.

### A Simple Solution

To remedy this H sync problem, a simple measure (shown in **Figure 3**) can be taken to change the H sync timing by adding a time-delay circuit, similar to the low-pass filter, to the H signal. Owing to the small difference of phase

between XCLK and H sync, the timing adjustment should be kept minimal. Furthermore, modifying the register for the change the timing will not be feasible as the timing step for the register is too big.

The value of  $R_T$  times  $C_T$  is proportional to the time delay we wish the TVHSYNC to have. Note that  $R_T$  is the sum of the wire resistance and  $R$ , and the output resistance of H in the TV encoder and  $C_T$  is the sum of  $C$  and the input capacitor load of TVSHYNC in the graphics controller. For the typical application,  $C$  can be 5 to 20 pF, and  $R$  can be 0 ~ 10  $\Omega$ .



**Figure 3: The treatment for H sync signal to add a small amount of delay.**

For the application of many display modes, thus using several frequencies, the delay approach may fail for some of modes. The problem arises from the fact that the delay can be too long or too short for a variety of frequencies and results in uncontrollable clocking edges.

Note that H sync is the only signal we try to alter. We shall not add a capacitor between P-OUT and TVCLKIN or between TVCLKOUT and XCLK. The adding will only give noise, not being able to perform the correct logic operations. If there exists a vertical sync problem, the addition of  $C$  may be employed. However, normally the phase change is negligibly small to create the problem.