PCB Layout and Design Considerations for CH7010 DVI/TV Output Device

Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7010 DVI/TV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video Components for both TMDS™ links and TV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for references. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of CH7010.

Component Placement

Components associated with the CH7010 encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

• Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors (C7, C8, C9, C11, C12, C14, C15, C17) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7010 ground pins, in addition to ground vias.

♦ Ground Pins

The analog and digital grounds of the CH7010 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7010 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

♦ Power Supply Pins

Separate digital (including the I/O supply voltage DVDDV), DVI, Analog, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment in CH7010

Pin Assignment	# of Pins	Type	Symbol	Description	Voltage Rating
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage**	**+3.3v**
6, 11, 64	3	Power	DGND	**Digital Ground**	
45	1	Power	DVDDV	**I/O Supply Voltage**	**+3.3v ~ +1.1v**
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage**	**+3.3v**
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**	
18, 44	2	Power	AVDD	**PLL Supply Voltage**	**+3.3v**
16, 17, 41	3	Power	AGND	**PLL Ground**	
33	1	Power	VDD	**DAC Supply Voltage**	**+3.3v**
34, 40	2	Power	GND	**DAC Ground**	

♦ DVDDV & VREF Decoupling and Connection

VREF is used as a reference level for pixel data input D[11:0], H sync input, V sync input, P-OUT output. For the optimum decoupling, please refer to **Figure 2**.

In general application, VREF is derived from DVDDV divided by 2, i.e., VREF = 1/2 × DVDDV. Therefore, in **Figure 2**, both resistors should have the same value (10KΩ@ 1%). The decoupling capacitor is required as shown in **Figure 2**. Also the DVDDV voltage supply should be connected to the graphics controller I/O VDD.

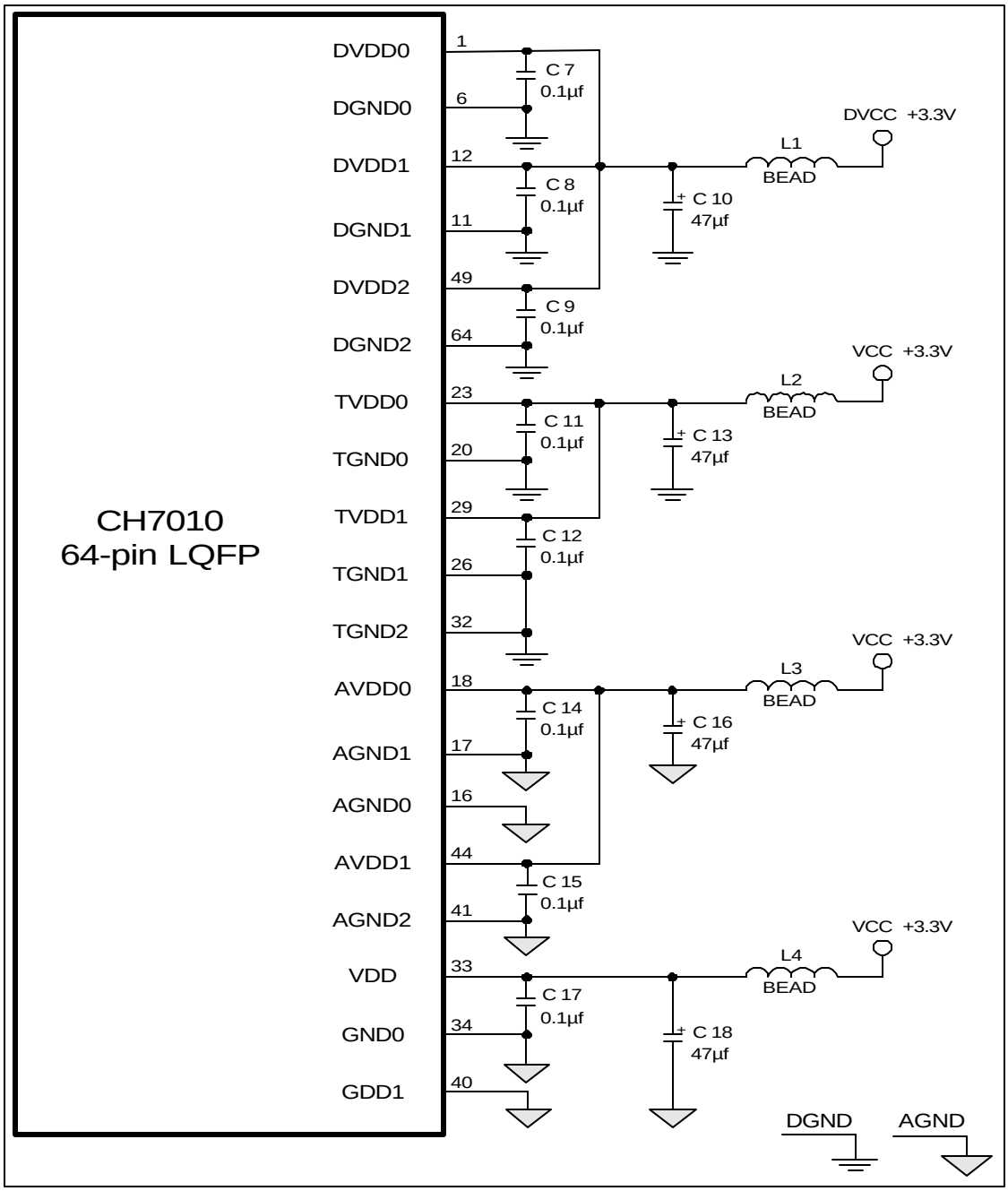


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have <.05ohm at DC; 23ohm at 25MHz & 47ohm at 100MHz. Please refer to Fair_Rite part# 2743019447 for detail or an equivalent part can be used for the diagram.

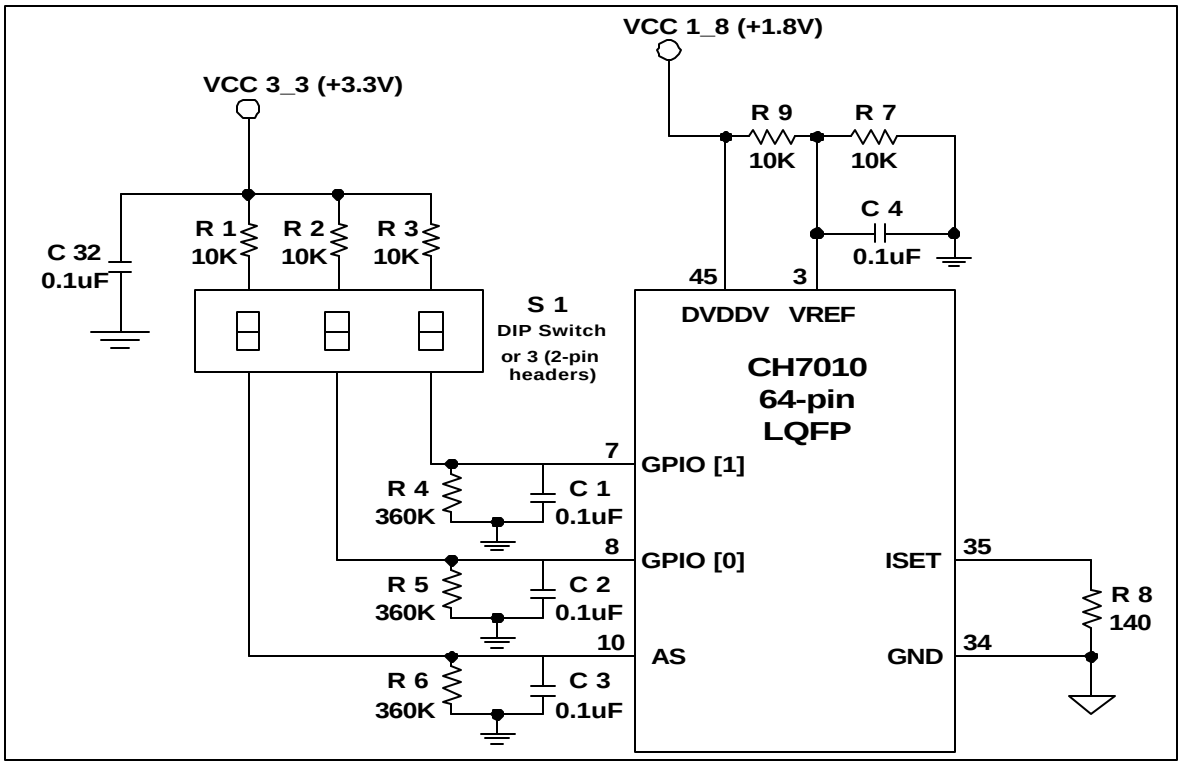


Figure 2: (1) ISET, VREF and DVDDV Connection; (2) GPIO and AS connection

• General Controls and Inputs

♦ ISET pin

A 140Ω resistor should be placed directly and as close as possible to Pin 35 with short and wide traces. Whenever possible, the ISET resistors ground pin should also be connected to the pin 34. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7010. See **Figure 2** for design reference.

♦ Data Enable pin

This pin (Pin 2) accepts a Data Enable signal which is high when active video data is input to the device, and low all other times. The voltage levels are between 0 and DVDDV, and the VREF signal is used as the threshold level. This input is used by the TMDS™ links and is not necessary for TV Out mode.

♦ GPIO [0] & GPIO[1] pins

In applications using Intel i815 or Intel i810 chipset* and the Intel software driver, it is recommended that the Pins 7 and 8 for GPIOs should be configured as shown in **Figure 2**. GPIO[0] is used to select NTSC (GPIO[0] = high) or PAL (GPIO[0] = low) in TV Out mode. GPIO[1] is used to select the output mode to be either TMDS™ links or TV video output. WhenGPIO[1] = high, the TV video output is selected, and GPIO[1] = low, the TMDS™ link monitor is selected.

♦ AS pin

In applications using Intel i815 or Intel i810 chipset* and the Intel software driver, it is recommended that the Pin 10 Address Select should be configured as shown in **Figure 2**. This pin determines the IIC address of the device is either 0x75 (AS= low) or 0x76 (AS= high).

♦ Horizontal and Vertical Sync Signals (HSYNC and VSYNC)

In input modes where the horizontal and vertical sync signals from the graphics controller are shared between the CH7010 and the computer monitor, buffering the sync signals prior to connecting them to the monitor is recommended (please refer to **Figure 3** below). These buffers help isolate any noise generated from the monitor connection (e.g., reflections, etc.) from coupling into the sync inputs of the CH7010, thereby degrading the display quality. In modes where the embedded syncs are used, these buffers are not necessary.

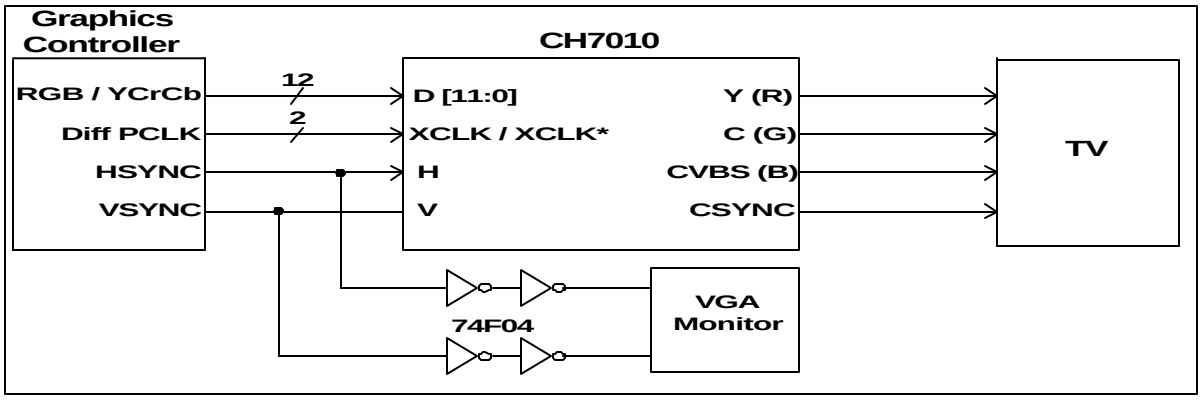


Figure 3: Sync Buffers

Note: If differential pixel clock from the graphics controller is not available, XCLK* should be tied to VREF.

♦ Video Inputs (D[0:11])

Since the digital pixel data and the pixel clock of the CH7010 may toggle at speeds up to 165MHz (depending on input mode), it is critical that the connection of these video signals between the graphics controller and the CH7010 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

♦ Pixel Clock Mode

Depending on the architecture and configuration of the graphics controller, CH7010 may have different clock modes settings. In all these modes, H sync, V sync and pixel data D[11:0] must meet the setup and hold time with respect to pixel clock.

♣ Master Clock Mode

When CH7010 is operated in TV Out mode, P-OUT/TLDET pin outputs a pixel clock to the graphics controller.

To set the Master Clock Mode for CH7010, Bit 3 of Register CM (1Ch) should set to 1. The 14.31818MHz clock is then used as a frequency reference in the TV PLL.

Bit 0 of register CM signifies the XCLK frequency. A value of 0 is used when the XCLK is at the pixel frequency (duel edge clocking mode) and a value of 1 is used when the XCLK is twice the pixel frequency (single edge clocking mode).

Bit 1 of register CM controls the P-OUT clock frequency. A value of 0 generates a clock output at the pixel frequency, while a value of 1 generates a clock at twice the pixel frequency.

Bit 2 of register CM controls the phase of the XCLK clock input to the CH7010. A value of 1 inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

The direction of H sync and V sync signal can be controlled by Sync Register 1Fh. When the bit5 (SYO) = 0, the Hsync and V sync signals are input to CH7010. When the bit5 (SYO) = 1, the H sync and V sync signals are output to graphics controller. It is recommended to configure CH7010 in this clock mode with SYO set to 0 when the application use with the Intel i815 or Intel i810 chipset* (See **Figure 4** for design details).

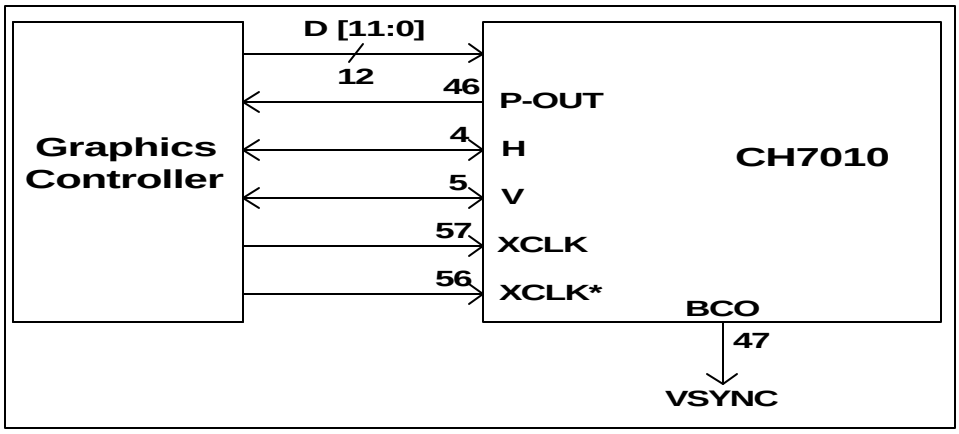


Figure 4: Master Clock Mode

♣ **BCO pin**

When BCO is used to provide a Buffered Clock Output, the output clock can be selected using BCO Register (22h). **Table 2** shows the details of the buffered output clock modes.

Table 2: BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	The 14MHz crystal	100	Sine ROM MSB
001	UCLK	101	Cosine ROM MSB
010	VCO divided by K3	110	VGA Vertical Sync
011	Field ID	111	TV Vertical Sync

♣ **Slave Clock Mode**

For this mode, select register 1Ch (Clock Mode Register, CM) bit 3 = 0. The pixel clock comes from the graphics controller and the P-OUT pin is in high impedance state (not automatically). The XCLK input is then used as a reference to the TV PLL. The direction of H sync and V sync signal can be controlled by Sync Register 1Fh. When the bit5 (SYO) = 0, the H sync and V sync signals are input to CH7010. When the bit5 (SYO) = 1, the H sync and V sync signals are output to graphics controller. It is recommended to configure CH7010 in this clock mode with SYO set to 0 when the application use with the Intel i815 or Intel i810 chipset* (See **Figure 5** for design details).

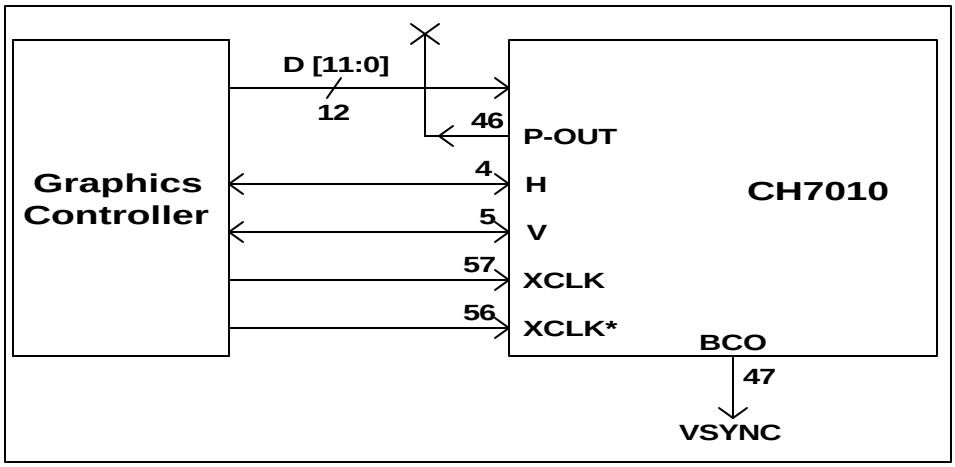


Figure 5: Slave Clock Mode

♣ **Embedded Sync Mode** (TV-Out only)

In order to enable this mode, Input Data Format Register 1Fh needs to be set for IDF = 4. Since H sync and V sync signals can be embedded into the data stream, the connections of H sync and V sync pins are not required between the graphics controller and CH7010. Please refer CCIR656 for details on how the H sync and V sync, odd field & even field signals are generated within the data stream (See **Figure 6** for design details for embedded sync in slave clock mode. Please note that the master clock mode can also be used.)

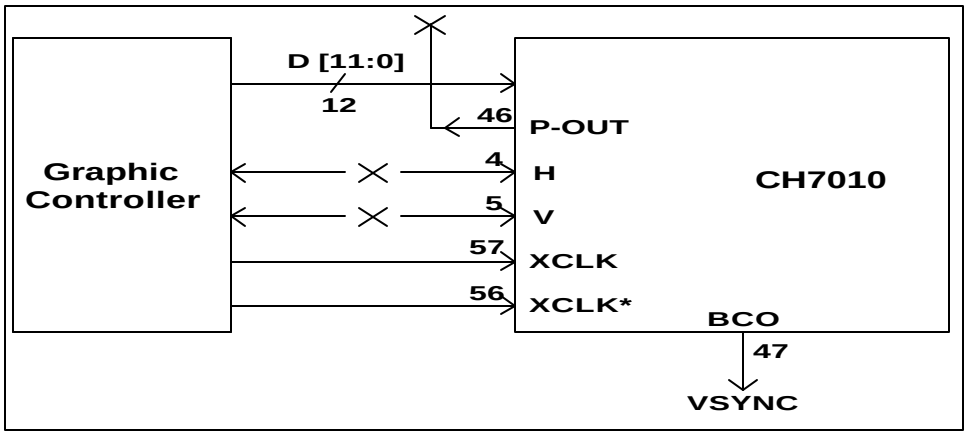


Figure 6: Embedded Sync (in slave clock) Mode

♦ Crystal Input

The 14.31818 MHz (±20ppm) crystal must be placed as close as possible to the XI/FIN and XO pins (Pins 42 and 43), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7010 encoder, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7010 pin 41 ground (See **Figure 7**).

♦ Reference Crystal Oscillator

The CH7010 includes an oscillator circuit which allows an inexpensive 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7010. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and posse low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

- Crystal is specified as 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance).
- Crystal is operated with a load capacitance equal to its specified value (C_L).
- External load capacitors have their ground connection very close to the CH7010 (C_{ext}).
- To allow tunability, a variable cap may be used from XI/FIN to ground.

Note that the XI/FIN and XO pin each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$

where:
C_{ext} = external load capacitance required on XI/FIN and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.
C_{int} = capacitance internal to CH7010 (approximately 10-15 pF on each of XI/FIN and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 7** for the symbols used in the calculation described above.

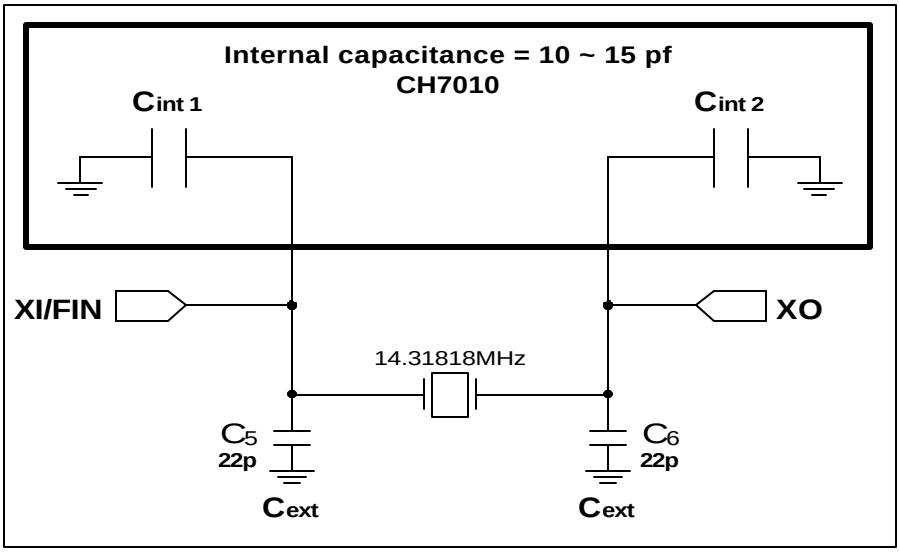


Figure 7: Reference Crystal

$$C_L = \frac{(C_{int\ XI/FIN} + C_{ext\ XI/FIN})(C_{int\ XO} + C_{ext\ XO})}{C_{int\ XI/FIN} + C_{int\ XO} + C_{ext\ XI/FIN} + C_{ext\ XO}} + C_S$$

In general , let us assume

C_{int} **XI/FIN** = C_{int} **XO** = C_{int}
C_{ext} **XI/FIN** = C_{ext} **XO** = C_{ext}

such that

$C_L = (C_{int} + C\ ext) / 2 + C_S$ and $C\ ext = 2 (C_L - C_S) - C_{int}$
$= 2 C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int}/2 + C_S$ in order to select C_{ext} properly.

Drive level

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in excessive drive level specified by crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

Drive level = 1/2 (2π f x C_L x V) ^{2} x R_S

R_S : Motion resistance in Ω. (< 50 Ω)
V : Operating voltage of crystal oscillator circuit.
f : Crystal operating frequency (14.31818 MHz).

For the detail consideration of crystal oscillator design, please refer AN-06.

• DVI Output and Control

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7010 from the graphics controllers digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

The TDC0, TDC1, TDC2 & TLC signals are high frequency differential signals that need to be routed with special precautions. Since the TDC0, TDC1, TDC2 & TLC signals are differential they must be routed in pairs: TDC0 & TDC0*, TDC1 & TDC1*, TDC2 & TDC2*, TLC & TLC* signals. The lengths of the 4 pair of signals must be kept as close to the same as possible. The maximum length difference must not euxceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the DVI connector without any vias to the bottom layer. The pin placement of the TDC0, TDC1, TDC2 & TLC signals allows for a direct route to the DVI connector.

The CH7010 comes in versions able to drive a DVI display at a pixel rate of up to 165 MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

Figure 8 shows an example of the connection of the DVI output. In the figure a DVI-I Right Angle Connector is used to interface the CH7010 DVI outputs to the monitor.

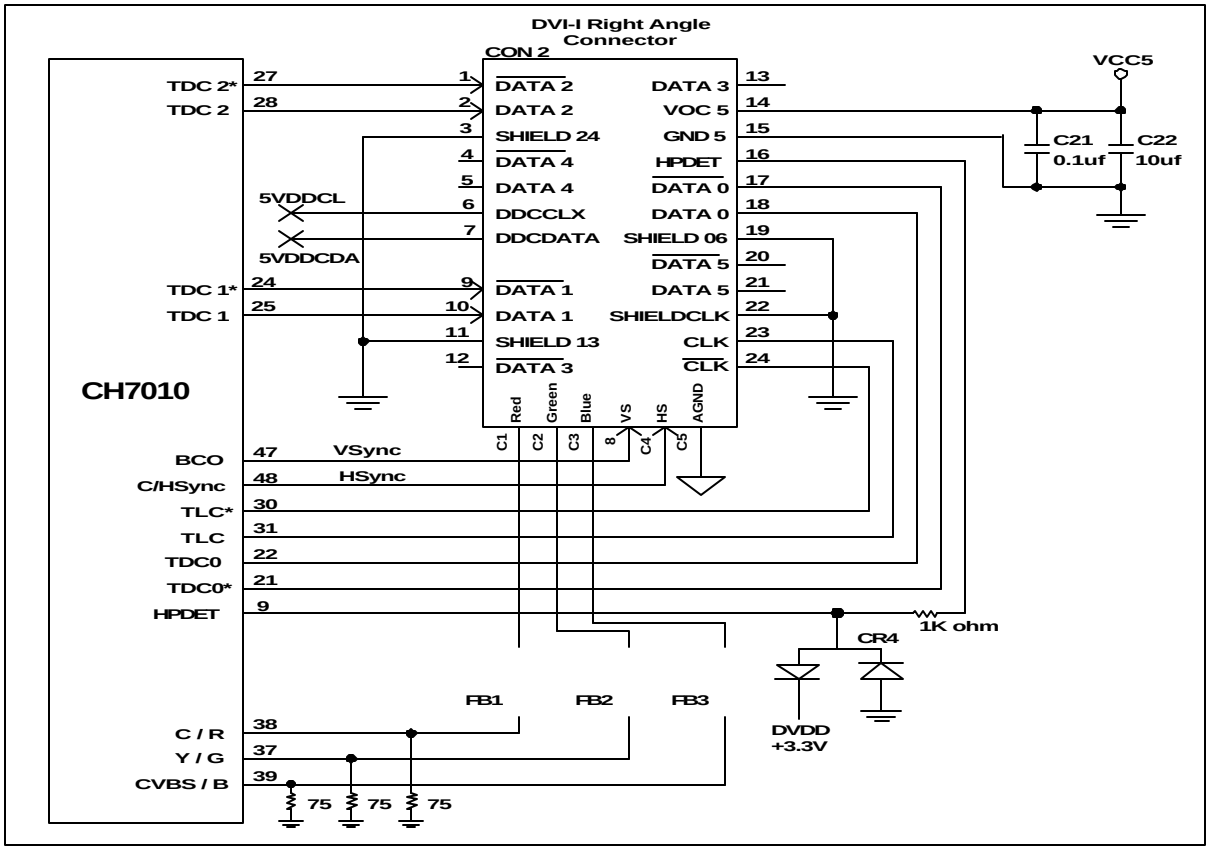


Figure 8: The connection of the DVI output

♦ TMDS™ Link Detect Output (TLDET*) (internal pull-up)

The TLDET* (Pins 7 and Pin 46) provides a general purpose I/O controlled via the IIC bus. No internal pull-up when TLDET* is selected. When the GPIO[1]/TLDET* pin is configured as an output, this pin can be used to output the TMDS™ link detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through IIC control (See **Figure 8**). Also there are two different pins within the CH7010 (pin 7 or pin 46) can be used to feed back to the graphics device when there has been a change in the state of the hot plug detect (HPDET) pin. Pin 7 is enabled when GOENB[1] is set high, and HPIE2 is set high. Pin 46 is enabled when POUTE is low, and HPIE is high. Whichever pin is enabled for the TLDET* function will pull low with an open drain output following a transition on the HPDET input.

♦ DVI Data Channel (TDC[0:2] and TDC[0:2]*)

These pins (Pins 22, 25, 28 for TDC[0:2] and Pins 21, 24, 27 for TDC[0:2]*) provide the DVI differential outputs for data channel 0 (blue), channel 1(green) and channel 2 (red) (See **Figure 8**).

♦ TMDS™ Link Clock Outputs (TLC and TLC*)

These pins (Pins 30, 31) provide the DVI differential clock outputs for the DVI interface corresponding to data on the TDC[0:2] outputs (See **Figure 8**).

♦ HPDET (DVI Hot Plug Detect)

This input pin (Pin 9) determines whether the TMDS™ link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the P-OUT/TLDET* or GPIO[1] TLDET* pin pulling low (See **Figure 8**).

♦ VSWING (TMDS™ Link Swing Control)

This pin (Pin 19) sets the swing level of the DVI outputs. A 2.4Kohm resistor should be connected between this pin and GND using short and wide traces.

♦ TV Video Outputs

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7010 from the graphics controller's digital output port. A P-OUT clock can be output as a frequency reference to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7010 from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. The modes supported for TV output are shown in the table below.

Table 3: TV Output Modes

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480[1]	4:3	9:8	NTSC	1/1
720x480[2]	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576[1]	4:3	15:12	PAL	1/1
720x576[2]	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

The components associated with the video output pins should be placed as close as possible to the CH7010. The 75Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7010 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended frequency response and the circuit elements are shown in **Figure 9** and **Figure 10**.

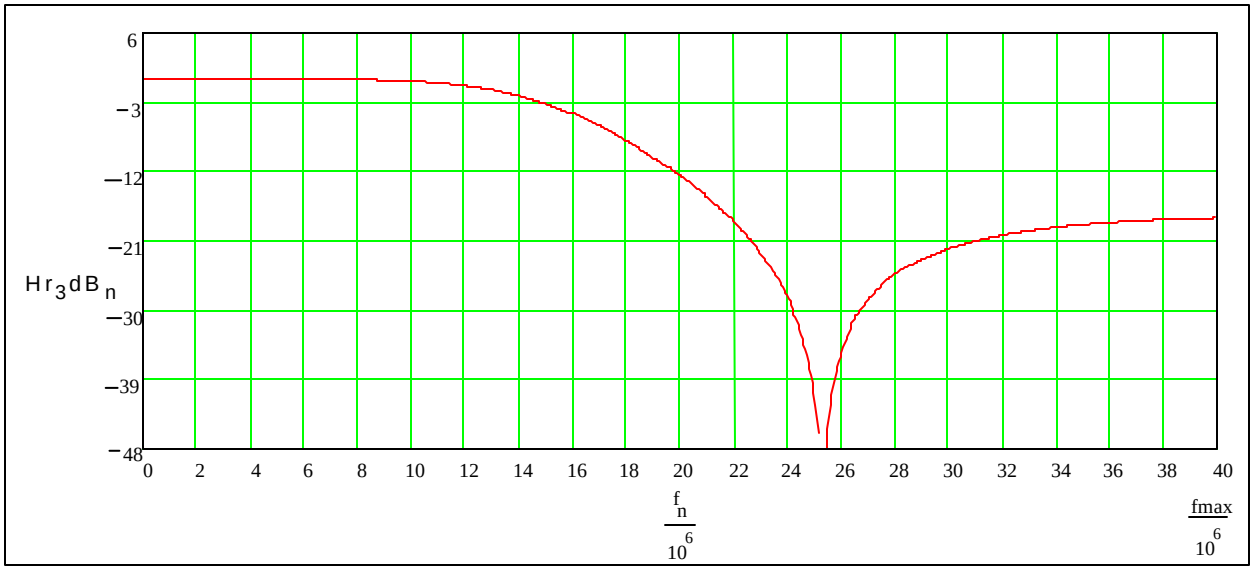


Figure 9: Amplitude Response of the 3rd Order Resconstruction Filter

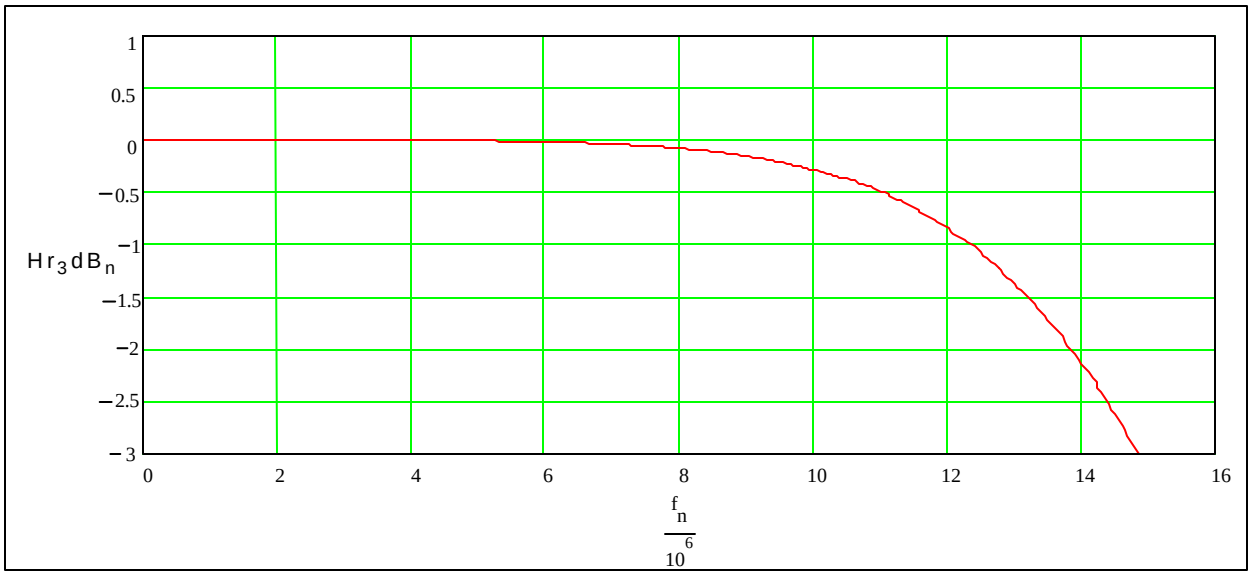


Figure 10: The Details of the Amplitude Response of the Pass Band

The output of the CH7010 may be configured for the following video output types: S-Video, composite, and SCART. **Figure 11** illustrates the typical connection for the S-Video and composite outputs, while **Figure 12** illustrates the connection for the SCART connector. For SCART arrangement 1, set FF Register (address 01h) bit 6 VOF = 1 and BL Register (address 07h) BL[7:0] = 0. For SCART arrangement 2, set VOF = 0 and BL[7:0] = 110, and CVBWB =0 (Register 02h bit 5).

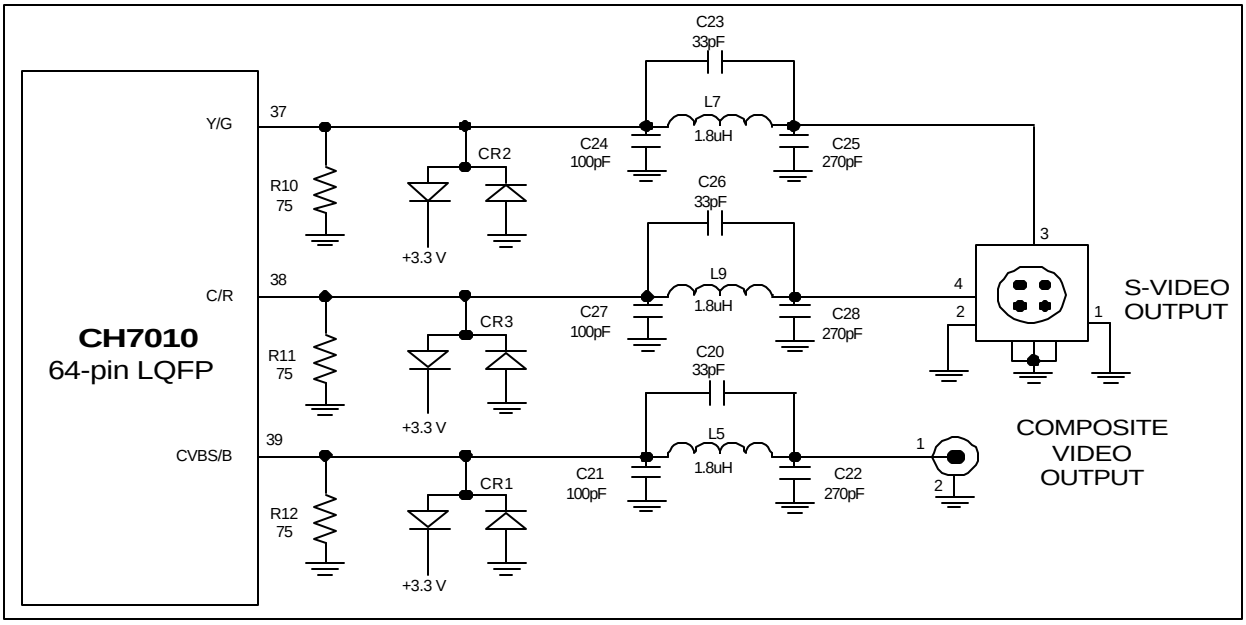


Figure 11: S-Video and Composite Video Outputs

Note: If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN27 on how to achieve the desire configuration.

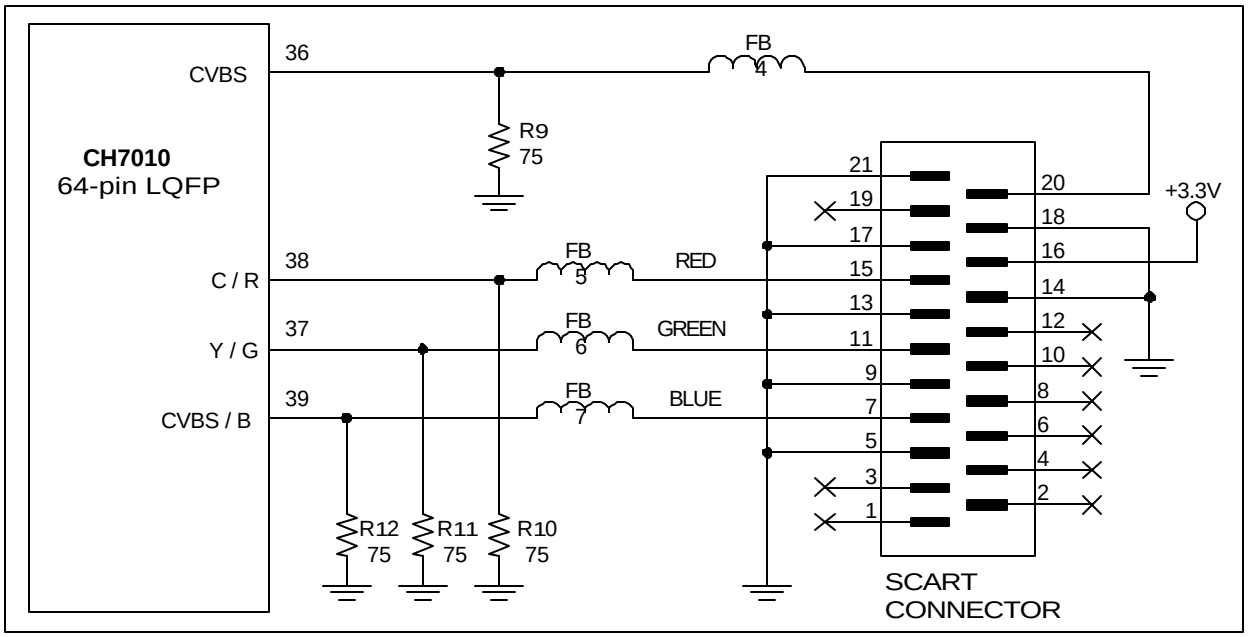


Figure 12: SCART Video Output

Careful layout consideration for the CVBS, Y/G, C/R & CVBS/B traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS should be separated with Ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not placed too close to each other.

The CVBS, Y/G, C/R & CVBS/B signals are analog video signals. These signals should be routed using 75 ohm traces. These signals should not be routed together with a minimum of 12 mil spacing between each other and 20 mil spacing between them and any digital trace.

Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corners should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them.

The input protection diodes CR1 - CR3 and the series termination resistors R10-R12 should be placed as close to the CH7010 as possible. The low pass filter networks should be placed as close to J1 and J2, the RCA and SVHS connectors as possible to reduce EMI emissions.

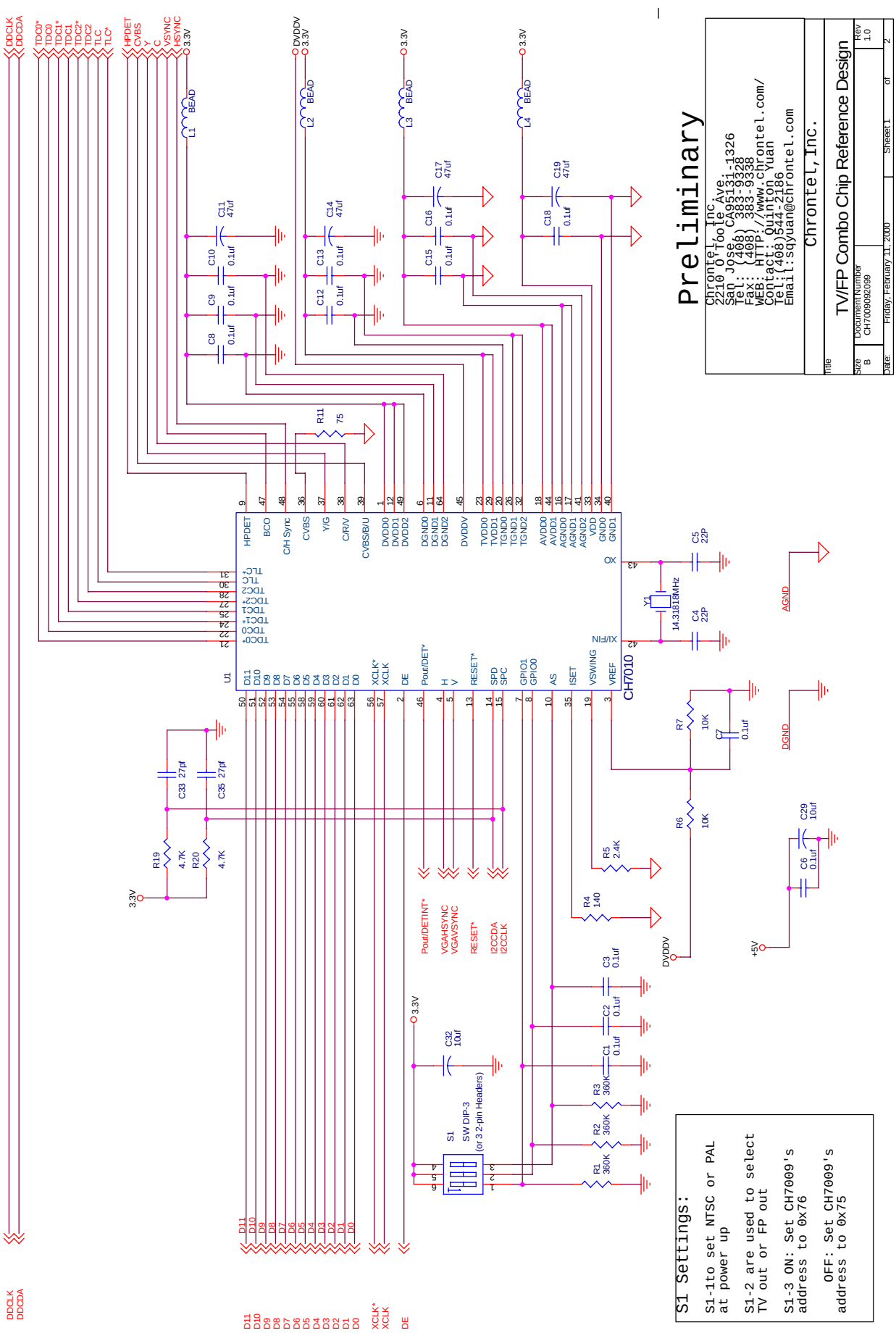
If the analog outputs of the DVI-I connector are to be used the ferrite beads FB1-FB3 should be placed as close to the DVI-I connector as possible to reduce EMI emissions.

Reference Design Example

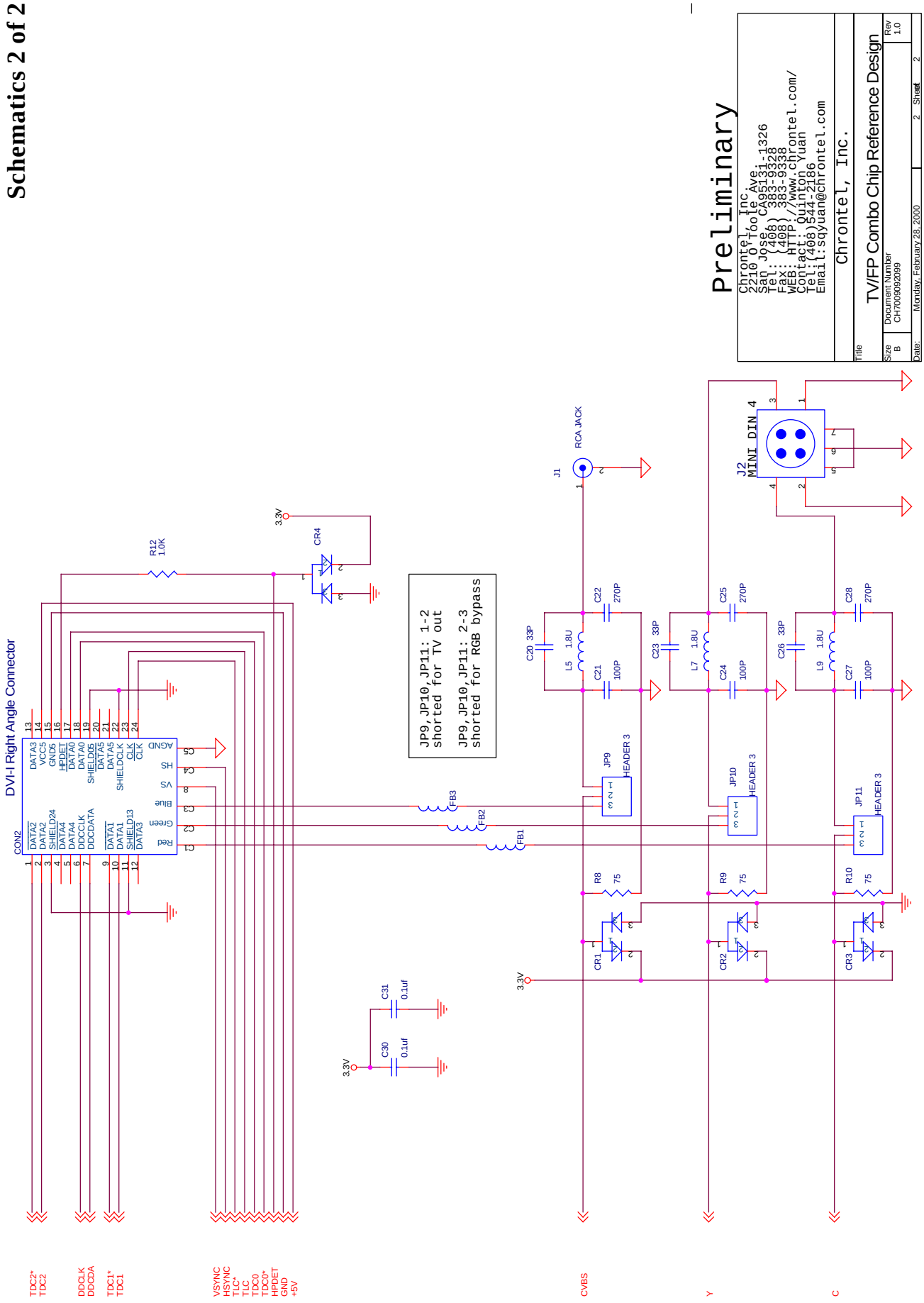
Attachments 1 and 2 show the schematics and PCB layout for a reference design for the CH7010 implementation to drive DVI monitor or TV video output.

Attachment 1. Reference Schematics for the implementation of CH7010

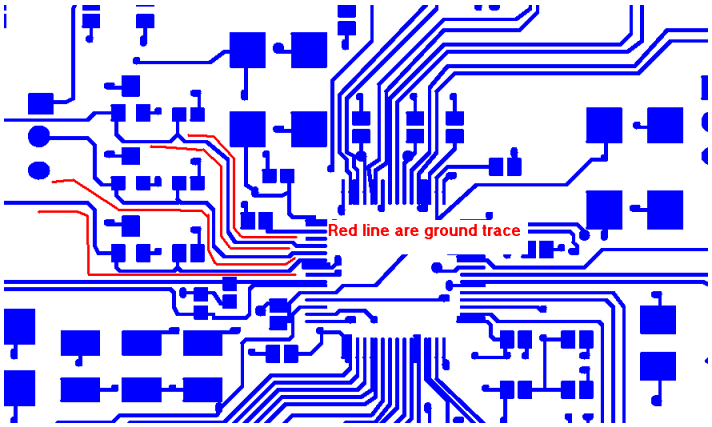
Schematics 1 of 2



Schematics 2 of 2



Attachment 2. PCB Layout for the CH7010 Reference Schematics



Primary Side

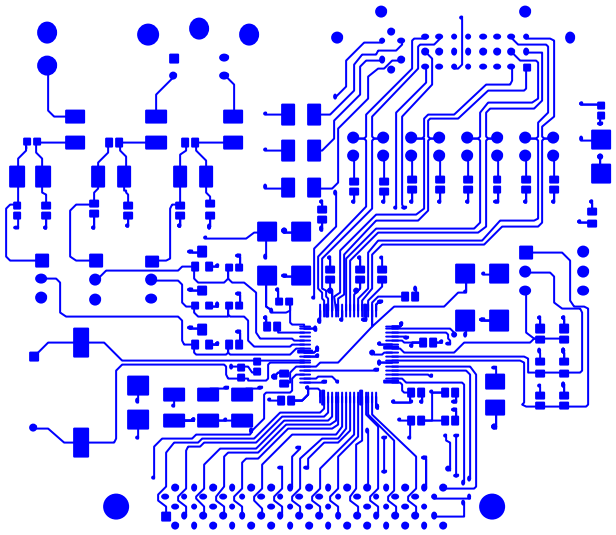
NOTES: UNLESS OTHERWISE SPECIFIED:

1. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.
2. FABRICATE PER INTEL 454979 CLASS 2.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
4. SMT LAND PATTERNS THAT HAVE A FINISHED PAD WIDTH RANGING FROM .012" to .015" MUST USE THE FOLLOWING TOLERANCE. +.002/-.0005.
   PCB VENDOR TO ADJUST ARTWORK TO COMPENSATE FOR ETCH PROCESS.

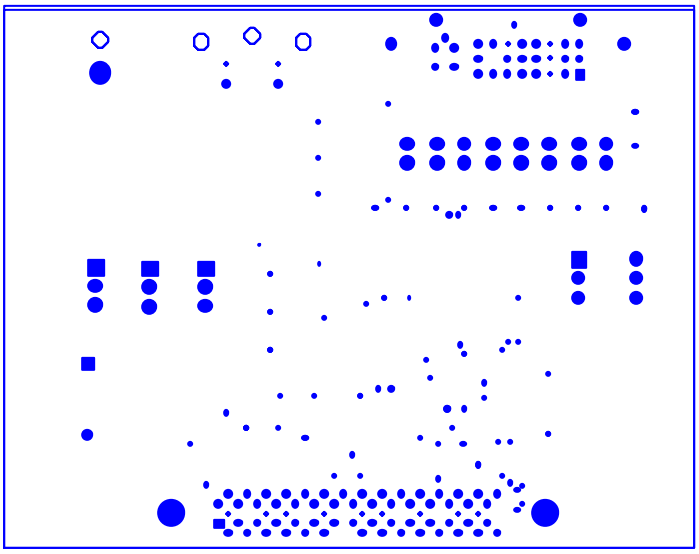
Note: Ground Plane is Duplicated

DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
◇	0.018		68	
○	0.020		55	
⏚	0.028		102	
×	0.034		6	
⊠	0.035		6	
△	0.037		6	
+	0.038		20	
⋈	0.042		3	
⊞	0.090		5	
○	0.125		2	NON-PLATED
TOTAL			273	

Layout 1 of 3

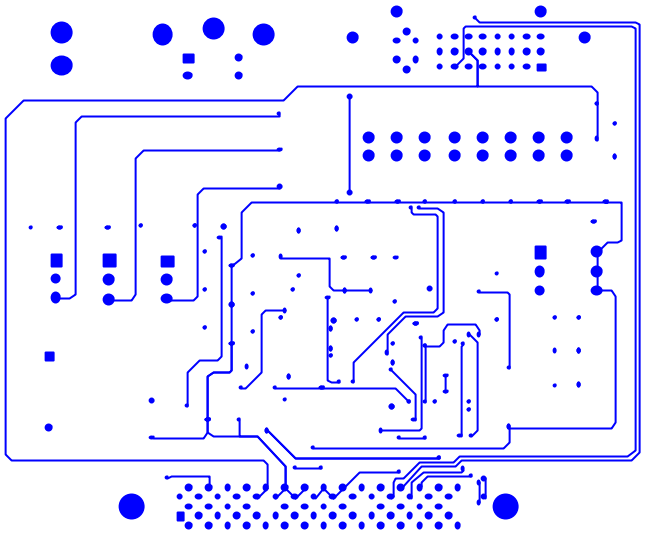


Top side

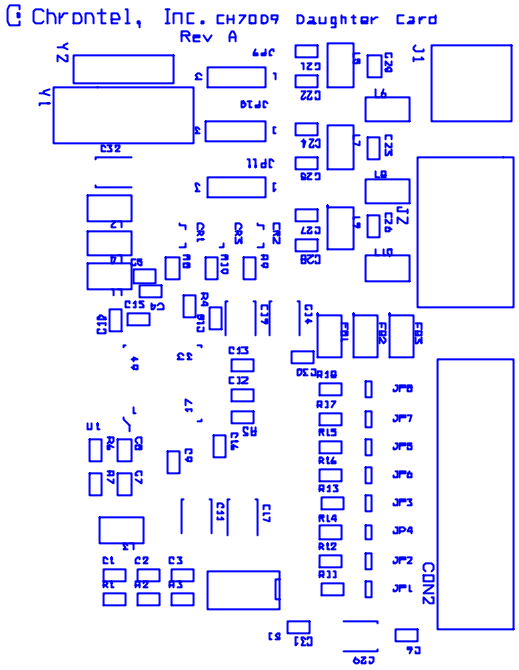


Ground side

Layout 2 of 3



Bottom side



Assembly top side

*** It is suggested that in order to prevent the DAC output from cross talk interference, the DAC output should be surrounded by grounding traces.**

Layout 3 of 3

CH7009/7010 BOM list

TV/FP Combo Chip Reference Design Revised: W			Tuesday, February 11,2000		
CH7009092099		Reversion 0.8			
Bill Of Materials		February 28,2000			
Item	Qty	Reference	Value	Part#	
1	1	CON1	DVO Connector / Right Angle	AMP# 536295-2	
2	1	CON2	DVI-I Vertical Receptacle	Molex # 74320-3004	
3	4	CR1,CR2,CR3,CR4	BAV99-DIO-SOT-23	Digi-Key# BAV99Z X CT-ND	
4	15	C1,C2,C3,C6,C7,C8,C9,C10,	0.1uf/16V 10% X 7R SMT 0603	Anchor# CAP0.1UFSMT-0603	
		C12,C13,C15,C16,C18,C30,C31			
5	2	C4,C5	22PF/50V 5% NPO SMT 0603	Digi-Key# PCC220ACVCT-ND	
6	4	C11,C14,C17,C19	47uf/20V Tant Size D	Mouser# 74-594DM16V47	
7	3	C20,C23,C26	33PF/50V 5% NPO SMT 0603	Digi-Key# PCC330ACVCT-ND	
8	3	C21,C24,C27	100PF/50V 5% NPO SMT 0603	Digi-Key# PCC101ACVCT-ND	
9	3	C22,C25,C28	270PF/50V 5% NPO SMT 0603	Digi-Key# PCC271ACVCT-ND	
10	2	C29,C32	10uf/20V 20% Y5V SMT 1210		
11	2	C33,C35	27PF/50V 5% NPO SMT 0603	Digi-Key# PCC270ACVCT-ND	
12	3	FB1,FB2,FB3	Bead Cores 1210 100MH 39ohm	Mouser# 436-3600	
13			JP1-JP8 removed		
14	3	JP9,JP10,JP11	HEADER 1x 3 single male	Digi-Key# W M2701-ND	
15	1	J1	RCA JACK	KLP-0848A-2	
16	1	J2	VIDEOJACK	Digi-Key# 275-1047-ND	
17	4	L1,L2,L3,L4	Ferrite Bead 1210	Digi-Key# 240-1038-1-ND	
18	3	L5,L7,L9	1.8UH 10% Ferrite SMT 1210	Digi-key# DN10182JCT-ND	
19					
20	3	R1,R2,R3	360K 1/16W 5% SMD 0603	Digi-Key# P360KGCT-ND	
21	1	R4	140 1/16W 5% SMD 0603	Digi-Key# P140GCT-ND	
22	1	R5	2.4K 1/16W 5% SMD 0603	Digi-Key# P2.4KGCT-ND	
23	2	R7,R6	10K 1/16W 5% SMD 0603	Digi-Key# P10KGCT-ND	
24	3	R8,R9,R10, R11	75 1/16W 5% SMD 0603	Digi-Key# P75GCT-ND	
25	1	R12	1.0K 1/16W 5% SMD 0603	Digi-Key# P1.0KGCT-ND	
26	2	R19,R20	4.7K 1/16W 5% SMD 0603	Digi-Key# P4.7KGCT-ND	