DVI OUTPUT EYE DIAGRAMS OF CH7009A/7301A VS. CH7009B/7301B

Scope

CH7009B/7301B, which are the successors of CH7009A/7301A, are fully DDWG compliant DVI transmitters. The new chips are able to transmit DVI display data from 25MHz up to 165 MHz pixel clocks. CH7009A/7301A is capable of transmitting data from 25 MHz to 135 MHz. A screened version of CH7009A/7301A would be able to support 165 MHz pixel clock if the DVI PLL is powered by 3.6V. This document gives a overall picture of what the DVI output eye-diagrams of CH7009A/7301A and CH7009B/7301B look like. The eye-diagrams of CH7009B/7301B support that these chips are versatile DVI transmitters with full compliance to DDWG specifications.

Eye-Diagrams of CH7009A/CH7301A

The DVI eye-diagram of some CH7009A/7301A chips may have uneven odd/even eyes when operating under high frequency modes. DVI resolutions such as the 1400 x 1050 pixels or 1600 x 1200 pixels, which require a pixel-clock frequency exceeding 135 MHz, may cause the uneven eye-diagram occurrence. As a result, pixel errors may occur. The uneven DVI eye-diagram comes from the post-VCO level-shifters within the DVI PLL. This phenomenon in CH7009A/7301A is an on-chip statistical processes problem, which has been fixed in the design of their successors, CH7009B/7301B.

Figure 1 shows an uneven odd/even eye-diagram from CH7009A/7301A chips at 162 MHz pixel clock frequency. From a design point of view, this chip should not be used at a frequency higher than 135MHz. A DC balanced duty-cycle screening process has been implemented to screen the CH7009A/7301A chips for running at a frequency up to 165 MHz. In order to retain good stability of the DVI PLL, the DVI PLL power (AVDD) is required to be 3.6V. **Figure 2** shows a well balanced eye-diagram at 162 MHz pixel clock from screened CH7009A/7301A chips. The eye-diagram is DDWG compliant.

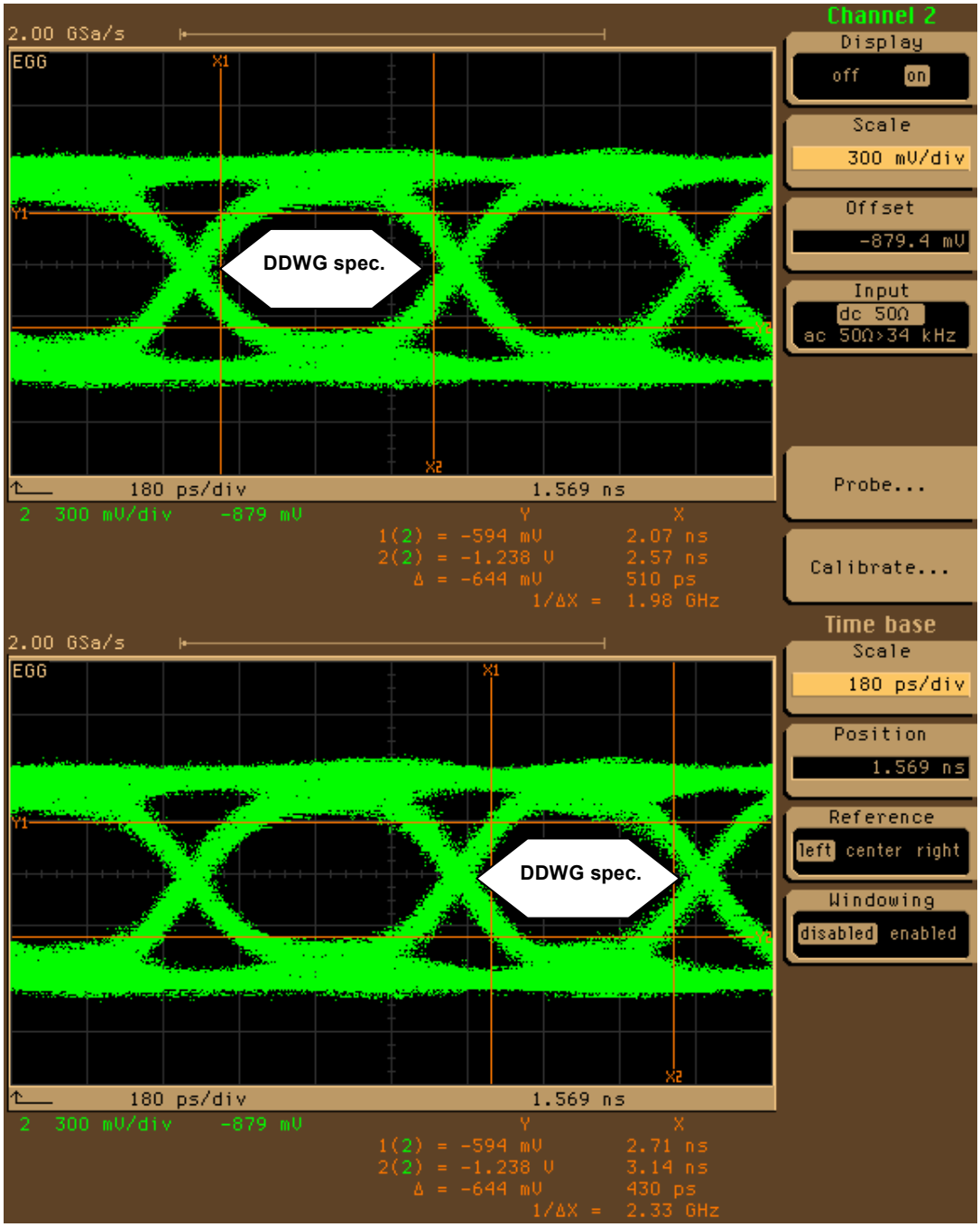

Figure 1: Eye-diagram of CH7009A/7301A DVI output at 162 MHz with 3.3V on DVI PLL Power Rail

The opening amplitude is 644mv and extreme horizontal openings are 510ps, and 430ps for the odd/ even eyes respectively. It complies with DDWG specification.

Figure 2: Eye-diagram of Screened CH7009A/7301A at 162 MHz with 3.6V on DVI PLL Power Rail

(Note: It is strongly recommended that the DVI power (AVDD) be 3.6V for pixel clock frequency higher than 135MHz)

The opening amplitude is 644mv and extreme horizontal openings are 470ps, and 470ps respectively. It complies with DDWG specification.

Eye-Diagrams of CH7009B/CH7301B

A new design of The DVI PLL has been implemented in CH7009B/7301B to correct the uneven eye-diagram problem and enhance the VCO speed. **Figure 3** shows a typical eye-diagram of CH7009B/7301B DVI output operating at 162MHz. The eye-diagram supports that the new chip is robust and is fully DDWG compliant.

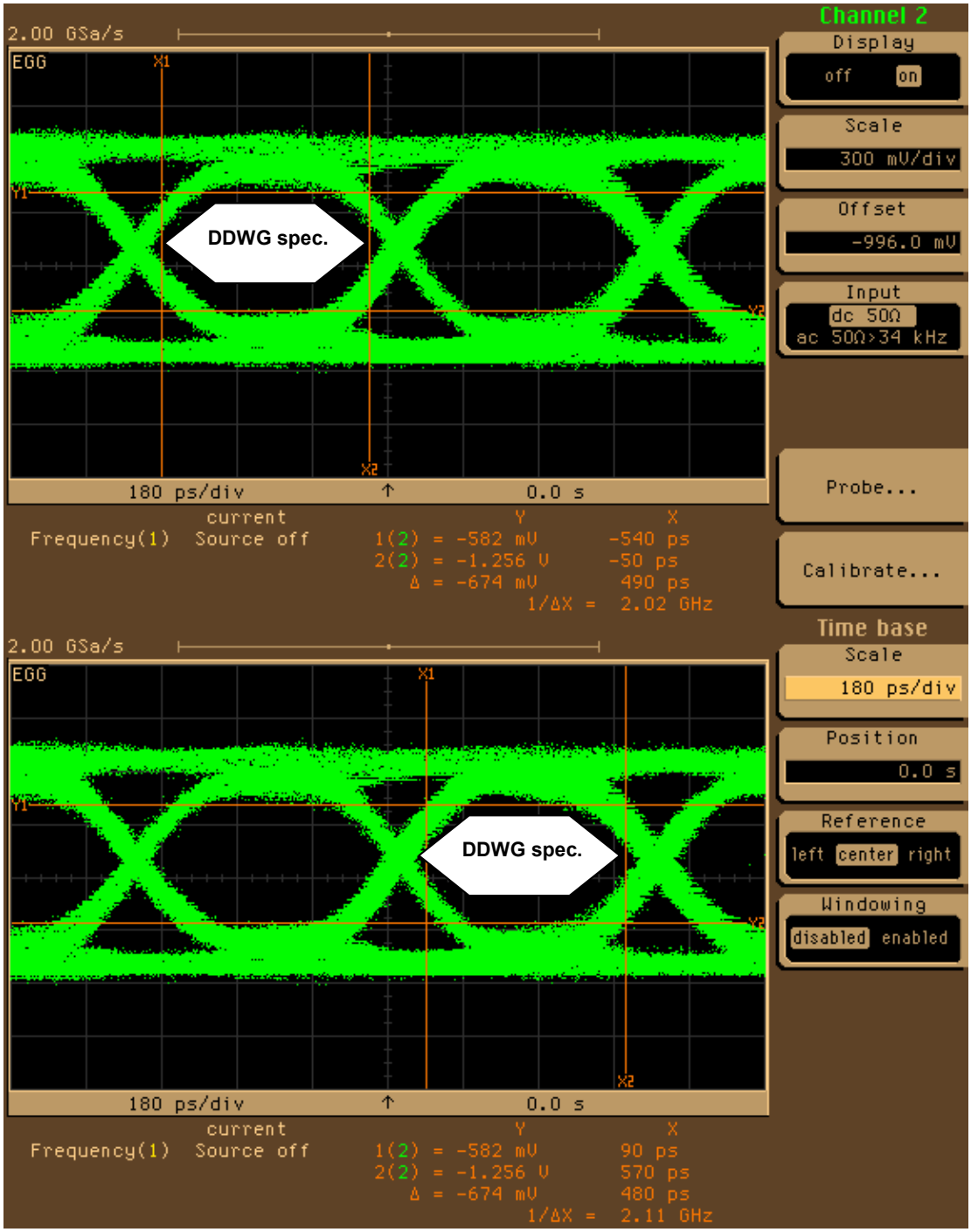

Figure 3: Eye-diagram of CH7009B/7301B at 162 MHz with 3.3V on DVI PLL Power Rail

The opening amplitude is 674mv and extreme horizontal openings are 490ps, and 480ps respectively. It complies with DDWG specification.

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